PATENT ABSTRACTS OF JAPAN

(11)Publication number : 07-183235
(43)Date of publication of application : 21.07.1995

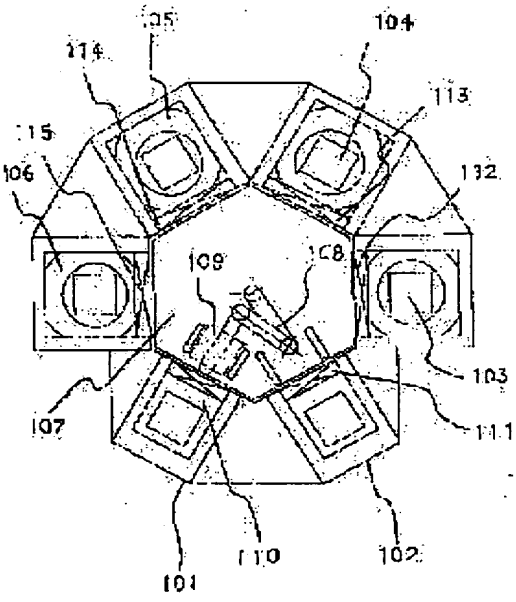
(51)Int.Cl. H01L 21/205
C23C 16/24
C23C 16/40
C23C 16/44
C23C 16/50
H01L 21/316
H01L 21/318

(21)Application number : 05-347646
(22)Date of filing : 24.12.1993

(71)Applicant : SEMICONDUCTOR ENERGY LAB CO LTD
(72)Inventor : OTANI HISASHI
SHIMADA HIROYUKI
SAKAMA MITSUNORI
ABE HISASHI

(54) MULTIPURPOSE SUBSTRATE TREATING DEVICE, ITS OPERATING METHOD, AND MANUFACTURE OF THIN FILM INTEGRATED CIRCUIT

(57)Abstract:
PURPOSE: To continuously perform various kinds of treatment, such as the formation of a thin film on a substrate, the annealing of the formed thin film, etc., while the airtightness is secured.
CONSTITUTION: A multipurpose substrate treating device is equipped with a transfer chamber 107 provided with a robot arm 108 for transferring substrates and multiple treating chambers 103-106 connected to each other through the chamber 107 and continuously perform a required treatment by transferring substrates 109 in and out from each treating chamber through the chamber 107. At least one of the treating chambers 103-106 has a silicon film manufacturing function using a low-pressure thermal CVD method and at least one of the remaining treating chambers has a silicon oxide film or silicon nitride film manufacturing function by plasma CVD method.



LEGAL STATUS

[Date of request for examination]	25.12.2000
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	withdrawal
[Date of final disposal for application]	14.01.2004
[Patent number]	

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] Have the processing room in which two or more reduced pressure is possible, and said two or more processing rooms are connected through the community room which can be decompressed. It has a means for conveying a substrate between each processing room in said community room. At least one of said two or more processing rooms is the multiple-purpose substrate processor characterized by membrane formation of the silicon film by the reduced pressure heat CVD being possible, and membrane formation of the oxidation silicon film by plasma CVD or a silicon nitride film being possible for at least one of said two or more processing rooms.
[Claim 2] Have the processing room in which two or more reduced pressure is possible, and said two or more processing rooms are connected through the community room which can be decompressed. It has a means for conveying a substrate between each processing room in said community room. Membrane formation of the silicon film by the reduced pressure heat CVD is possible for at least one of said two or more processing rooms, and membrane formation of the oxidation silicon film by plasma CVD is possible for at least one of said two or more processing rooms. At least one of said two or more processing rooms is the multiple-purpose substrate processor characterized by membrane formation of the silicon nitride film by plasma CVD being possible.
[Claim 3] Have the processing room in which two or more reduced pressure is possible, and reduced pressure **** is connected for said two or more processing rooms through the community room. In the condition of being the approach of a multiple-purpose substrate processor with the means for conveying a substrate between each processing room in said community room of operation, and having been held at the same pressure The substrate held at the community room is transported [transporting the substrate held at any one processing room to a community room, or] to any one processing room, And the approach of the multiple-purpose substrate processor characterized by to form the silicon film with the reduced pressure heat CVD in at least one of said processing rooms, and performing membrane formation of the oxidation silicon film or a silicon nitride film by plasma CVD in at least one of said processing rooms of operation.
[Claim 4] Have the processing room in which two or more reduced pressure is possible, and reduced pressure **** is connected for said two or more processing rooms through the community room. In the condition of being the approach of a multiple-purpose substrate processor with the means for conveying a substrate between each processing room in said community room of operation, and having been held at the same pressure The substrate held at the community room is transported [transporting the substrate held at any one processing room to a community room, or] to any one processing room, And the thing for which the silicon film is formed with the reduced pressure heat CVD in at least one of said processing rooms, And the approach of the multiple-purpose substrate processor characterized by to form the oxidation silicon film by plasma CVD in at least one of said processing rooms, and forming a silicon nitride film by plasma CVD in at least one of said processing rooms of operation.
[Claim 5] It is the production approach of the thin film integrated circuit which the process which carries out multilayer membrane formation including a silicon semi-conductor layer, the process which forms gate dielectric film, and the process which forms an interlayer insulation film are processed using the multiple-purpose substrate processor which has two or more reaction containers, and the inner silicon semi-conductor layer of said process is produced by the reduced-pressure heat CVD, and is characterized by what the inner gate-dielectric-film layer of said process was produced for by plasma CVD.
[Claim 6] Have the processing room in which two or more reduced pressure is possible, and said two or more processing rooms are connected through the community room which can be decompressed. The process which is the production approach of the thin film integrated circuit using a multiple-purpose substrate processor with

the means for conveying a substrate between each processing room in said community room, and forms a silicon nitride film by plasma CVD at the 1st processing room, The production approach of a thin film integrated circuit of having the process which forms the oxidation silicon film by plasma CVD at the 2nd processing room, the process which forms the silicon film with a reduced pressure heat CVD method at the 3rd processing room, and the process which forms oxidized-form membrane formation at the 4th processing room.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the equipment which forms in a substrate top or a substrate front face the semiconductor device which consists of polycrystal silicon. It is related with the equipment which can perform a process with the need put especially to the open air of being continuously carried out without ******. Moreover, it is related with the multiple-purpose substrate processor which can be used for production of a thin film integrated circuit.
[0002]
[Description of the Prior Art] The integrated circuit using a semi-conductor substrate or a glass substrate is known. IC and LSI are known as the former and the liquid crystal display of an active-matrix mold is known as the latter. In order to form such an integrated circuit, it is necessary to perform various processes continuously. For example, if it is the case where an insulated-gate mold electric field effect semiconductor device is formed, to form continuously is desired, without taking out outside the semiconductor region in which a channel is formed, and the gate dielectric film formed in contact with it. Moreover, it is the industry top need to perform various processes continuously efficiently.
[0003] Although it was desirable to these manufactures to perform a membrane formation process continuously within one equipment, the equipment with which only the manufacturing installation aiming at the manufacturing installation aiming at the semiconductor device with which the conventional manufacturing installation used amorphous silicon, or the semiconductor device using single crystal silicon existed but with which it was suitable for the semiconductor device using polycrystal silicon, and the manufacture approach using it were not established.
[0004]
[Problem(s) to be Solved by the Invention] This invention aims at offering the substrate processor which can process continuously the various processes needed for production of a semiconductor device which used polycrystal silicon with one equipment and which can be used for multiple purposes. In order to produce the semi-conductor especially using polycrystal silicon with a sufficient property, it is an indispensable configuration in said substrate processor that it is possible to form the insulator layer which needs to be prepared in contact with either [its] both to have the means forming of the silicon film by the reduced pressure heat CVD which used polysilane, or its upper and lower sides by plasma CVD.
[0005]
[The means for heating a technical problem] In order to produce the semiconductor device which has the barrier layer which consists of polycrystal silicon with a sufficient property, the multiple-purpose substrate processor of this invention Have the processing room in which two or more reduced pressure is possible, and said two or more processing rooms are connected through the community room which can be decompressed. It has a means for conveying a substrate between each processing room in said community room. Membrane formation of the silicon film by the reduced pressure heat CVD is possible for at least one of said two or more processing rooms, and membrane formation of the oxidation silicon film by plasma CVD or a silicon nitride film is possible for at least one of said two or more processing rooms, Or have the processing room in which two or more reduced pressure is possible, and said two or more processing rooms are connected through the community room which can be decompressed. It has a means for conveying a substrate between each processing room in said community room. Membrane formation of the silicon film by the reduced pressure heat CVD is possible for at least one of said two or more processing rooms, and membrane formation of the oxidation silicon film by plasma

CVD is possible for at least one of said two or more processing rooms. At least one of said two or more processing rooms is characterized [the / biggest] by membrane formation of the silicon nitride film by plasma CVD being possible.

[0006] In order to produce the semiconductor device which has the barrier layer which consists of polycrystal silicon with a sufficient property, moreover, the approach of the multiple-purpose substrate processor of this invention of operation In the condition of having been held at the same pressure, the substrate held at any one processing room is transported to a community room, Or the thing for which the substrate held at the community room is transported to any one processing room, And the thing for which the silicon film is formed with the reduced pressure heat CVD in at least one of said processing rooms, And the thing for which plasma CVD performs membrane formation of the oxidation silicon film, or membrane formation of a silicon nitride film in at least one of said processing rooms Or the thing for which the substrate held at any one processing room is transported to a community room in the condition of having been held at the same pressure, Or the thing for which the substrate held at the community room is transported to any one processing room, And the thing for which the silicon film is formed with the reduced pressure heat CVD in at least one of said processing rooms, And it is characterized [the] especially by the thing for which a silicon nitride film is formed by plasma CVD in at least one of forming the oxidation silicon film by plasma CVD in at least one of said processing rooms, and said processing rooms.

[0007] If the need of taking the above configurations is described briefly, the manufacture process of a semiconductor device of having used amorphous silicon will have been conventionally used for manufacture of the semiconductor device using polycrystal silicon chiefly. The plasma CVD which used glow discharge is used for membrane formation of the silicon film in that case. The silicon film produced by making it the appearance contains a lot of hydrogen, and a membranous condition changes a lot with emission of the hydrogen at the time of making it crystallize etc. It became clear that it is difficult to obtain the semiconductor device which consists a configuration like continuation membrane formation which had many processing rooms with much trouble of polycrystal silicon which has very sufficient property as a result of the experiment. In order to solve this trouble, it turned out using LPCVD that it is effective to use the polysilane like a disilane as material gas.

[0008] However, in an existing manufacturing installation and an existing manufacture process, since it was once exposed into atmospheric air even if it is the case where LPCVD is used, it was difficult to obtain the semiconductor device which consists of polycrystal silicon which cannot form an interface with a sufficient property but has too sufficient property. So, in order to realize junction of the most important, beautiful interface, it is forming membrane formation of the silicon film by LPCVD, and the insulator layer which needs to be prepared in contact with both the upper and lower sides or one of these, without opening to atmospheric air continuously, and it became clear by experiment of artificers for the fast improvement in a property to be possible. As the membrane formation approach of this insulator layer, the conclusion that the approach by plasma CVD was the best was reached in consideration of the property, the throughput, etc. from artificers' experimental result.

[0009] The concrete example of this invention is shown in drawing 1 . The equipment shown in drawing 1 can be used for multiple purposes, and can be combined by the number which needs the processing room which performs membrane formation to need and annealing treatment. A glass substrate, a silicon substrate, other insulating substrates, and a semi-conductor substrate can be used as a substrate processed with the equipment shown in drawing 1 . That is, if it is the substrate which has an insulating front face, it can use. For example, if it is electro-optic devices, such as a liquid crystal display of a active-matrix mold, and image sensors, it is common to use a cheap glass substrate.

[0010] For example, 107 is made into the conveyance room of the substrate which is a community room, 101 and 102 are made into a spare room among the processing rooms which perform various processings of a substrate, one side is used for carrying in of a substrate, and other one side is used for taking out of a substrate. Moreover, the configuration that 103 considers as the plasma-CVD equipment for forming an insulator layer, uses 104 as the reduced pressure heat CVD system for forming amorphous silicon, uses 105 as the heating furnace for forming the thermal oxidation film, and considers as the annealing furnace for performing annealing according 106 to an optical exposure can be taken. In addition, a spare room can also be called processing room for the purpose of having the function to perform carrying in and taking out of a substrate.

[0011] Such a combination can be performed to arbitration. As an element which can do these combination, plasma CVD, the reduced pressure heat CVD (in this specification, it abbreviates to LPCVD below), Light CVD, microwave CVD, a heating furnace, the annealing furnace by optical exposure, sputtering, plasma annealing, and

plasma etching can be mentioned.
[0012]
[Example]
[Example 1] The configuration of this example is shown in drawing 1 . In this example, 101 and 102 are spare rooms and it has the function to take a substrate in and out. These chambers have the function to hold the cassette by which two or more substrates were stored. Moreover, naturally in the introductory means of inert gas, the introductory means of cleaning gas, and the pan, it has the flueing means.
[0013] 103-106 are processing rooms, 103 and 106 are plasma-CVD equipment, and 104 is a temperature control chamber. A temperature control chamber has the function to heat a substrate to predetermined temperature, and in advance of membrane formation by other chambers, it is used in order to heat the substrate beforehand. The specification of each processing room is shown in the following table 1.
[0014]
[Table 1]

	106	105	104	103
処理内容	PCVD	予備加熱 RTP	PCVD LPCVD	PCVD
RF電源	13.56MHz 500 W	———	13.56MHz 500 W	13.56MHz 500 W
電　極	平行平板	平行平板	平行平板	平行平板
プロセスガス	N_2, SiH_4, NH_3 $Al(CH_3)_3$	N_2O, N_2, NH_3, O_2	N_2, SiH_4, H_2 Si_2H_6, Si_3H_8	N_2, TEOS, O_2 C_2F_6
クリーニングガス	NF_3 +N_2	———	NF_3 +N_2	NF_3 +N_2
基板加熱温度	450℃	450℃	550℃	600℃
膜	Si_2H_4 AlN	———	Si	SiO_2 SiF_x
排気設備	到達圧力 5×10^{-2}Torr	到達圧力 5×10^{-2}Torr	到達圧力 5×10^{-5}Torr	到達圧力 5×10^{-2}Torr

尚、基板サイズとしては、4インチ角、5インチ角、5×6インチ角を利用することができる。

[0015] 107 is the conveyance room of a substrate and a substrate has between each chamber conveyed by the robot arm 108. The robot arm 108 has the function for which takes out one substrate (shown by 109) at a time from a spare room 101 or 102, and it is moved to the reaction chamber to need. Naturally a substrate can be moved between each processing room. Moreover, the exhaust air means is formed also in this conveyance room, and it can be made the degree of vacuum to need.
[0016] Migration of the substrate between each chamber is performed by [as being the following]. For example, the substrate held in a spare room 101 is processed at the processing rooms 103 and 104, and the case where it carries in to a spare room 102 is considered. In this case, first, the (1) spare room 101 and the conveyance room 107 are made into the same reduced pressure condition (a high vacuum condition is desirable), a gate valve 110 is opened in that condition, and a substrate 109 is taken out in a conveyance room by the robot arm 108. A gate valve 110 is shut after that.
(2) Make the conveyance room 107 and the processing room 103 into the same reduced pressure condition, open a gate valve 112 in the condition, and carry in to a process room the substrate 109 held at the robot arm 108. A gate valve 112 is shut after that.
(3) A predetermined process is performed at the processing room 103.
(4) Make the degree of vacuum of the processing room 103 into the same reduced pressure condition as the conveyance room 107 after process ending at the processing room 103, open a gate valve 112 after that, and take out a substrate in the conveyance room 107 by the robot arm 108. And a gate valve 112 is shut.
(5) Make the conveyance room 107 and the processing room 104 into the same reduced pressure condition, open a gate valve 113 in the condition, and carry in to the processing room 104 the substrate held at the robot

arm 108. A gate valve is shut after that.
(6) A predetermined process is performed at the processing room 104.
(7) Make the degree of vacuum of the processing room 104 into the same reduced pressure condition as the conveyance room 107 after process ending at the processing room 104, open a gate valve 113 after that, and take out a substrate in the conveyance room 107 by the robot arm 108. And a gate valve 113 is shut.
(8) Make the conveyance room 107 and a spare room 102 into the same reduced pressure condition, open a gate valve 111 in the condition, by the robot arm 108, carry in a substrate to a spare room 102 and shut a gate valve 111 after that.
[0017] Processing beyond 2 times or it can be performed continuously, without putting one substrate to the open air as mentioned above. It is useful that not only membrane formation but annealing etc. can be performed as these processings.
[0018] The above (1) By repeating the process of – (8), two or more substrates held at the cartridge carried in to the spare room 101 can be continuously processed from a degree to a degree. And the substrate which processing ended will be held automatically at the cartridge of a spare room 102. Moreover, in the above-mentioned membrane formation process, down stream processing which continued while cleaning can be performed, without stopping the whole actuation by cleaning the processing room 104, and cleaning the processing room 103 conversely, while the processing room 104 works, while the processing room 103 works. As such cleaning, it is NF3. The plasma cleaning in the chamber to depend can be mentioned.
[0019] [Example 2] The example which produces the thin film integrated circuit which has at least one TFT which makes polycrystal silicon a barrier layer using the multiple-purpose membrane formation equipment shown in drawing 1 is shown in drawing 2 . First, the multiple-purpose membrane formation equipment used in this example is explained. In this example, 101 and 106 were made into the spare room, in order to perform carrying-in taking out of a substrate. 106 were especially carried out for 101 to substrate taking out for substrate carrying in here. Moreover, the RAPITTO thermal annealing process according 104 to the short-time exposure of infrared light (it is called RTA or RTP), Or it considers as the processing room which forms the film (nitriding aluminum oxide is called alumimium nitride below) or silicon nitride film which considers as the processing room which performs preheating and uses alumimium nitride as a principal component for 103 by the plasma-CVD method. the processing room which uses TEOS as a raw material for 104, and forms the oxidation silicon film by the plasma-CVD method -- carrying out -- 105 -- LPCVD -- it considers as the processing room which forms the amorphous silicon film by law. Moreover, the gas installation means for introducing the exhaust air means for changing each processing room into a reduced pressure condition and the gas needed further is formed in each processing room.
[0020] A making process is shown below. First, the glass substrate (a 4 inch angle, a 5 inch angle, or 5x6 inch angle) 201 of Corning 7059 grade is carried in to a spare room 101 as a substrate, and vacuum suction is carried out enough. As for this vacuum suction, it is desirable to carry out until it becomes the almost same pressure as the conveyance room 107 enough carried out in vacuum suction. And a gate valve 110 is opened and the substrate in a spare room 101 is transported to the conveyance room 107 by the robot arm 108. In drawing 1 , the substrate 201 in drawing 2 is shown as 109. In addition, it is called a substrate also including the film currently formed on it below. And the gate valve 112 between the reaction chambers 103 where vacuum suction was similarly mostly carried out to the same pressure is opened, and a substrate is carried in. A gate valve 112 is shut after substrate carrying in, and the alumimium nitride film 202 with a thickness of 2000-5000A is formed by the plasma-CVD method in this reaction chamber 103. Membrane formation is aluminum (C four H9)3. Or aluminum3 (CH3) N2 It carries out by using. Moreover, minute amount addition of the N2 O may be carried out, and thermal-expansion distortion may be made to ease.
[0021] After membrane formation of the alumimium nitride film 202 carries out vacuum suction of the reaction chamber 103 to the same degree of vacuum as the conveyance room 107. And a gate valve 112 is opened and a substrate is transported for a substrate to a conveyance room by the robot arm 108. Next, a substrate is carried in to the annealing chamber 104 where vacuum suction was similarly carried out. In this annealing chamber 104, RAPITTO thermal annealing (RTA) by infrared exposure is performed. This annealing is performed in the ambient atmosphere of nitrogen, ammonia (NH3), or nitrous oxide (N2 O), and heats the alumimium nitride film quickly for a short time. By this annealing, the alumimium nitride film becomes transparent and its insulation and thermal conductivity of that improve. Moreover, in order to prevent the penetration to the semi-conductor of impurities, such as NATORYUMU from a glass substrate, a silicon nitride film may be formed. In this case, it is a silicon nitride film by the plasma-CVD method The substrate temperature of 350 degrees C, 0.1Torr, and SiH4 NH3

Membranes are formed in a mixed ambient atmosphere.
[0022] And vacuum suction of the reaction chamber 104 is carried out, and a substrate is transported to the conveyance room 107 where vacuum suction was carried out again by the robot arm 108. And a substrate is conveyed to the reaction chamber 106 where vacuum suction was similarly carried out. In this reaction chamber 106, the oxidation silicon film 203 is formed by the plasma-CVD method which used TEOS as the raw material. Membrane formation conditions are shown below.
TEOS/O2 =10 / 100sccmRF power Whenever [350 W-set board temperature] 400-degree-C membrane formation pressure 0.25 Torr, it sets for the above-mentioned reaction and is C two F6 again. It adds and is SiOFx. The film shown may be formed.
[0023] This oxidation silicon film is formed as a substrate oxide film 203 by 2000-50A in thickness in the field which forms TFT. The oxidation silicon film 203 formed in this reaction chamber 106 may be conveyed to an annealing chamber 104, and RAPITTO thermal annealing may be performed.
[0024] And a substrate is again conveyed in the conveyance room 107, and then a substrate is carried in to a reaction chamber 105. All the things that a conveyance room and each processing room make open and close a gate valve in the case of migration of these substrates after vacuum suction is carried out to the same degree of vacuum (the same reduced pressure condition) are common.
[0025] a reaction chamber 105 -- LPCVD -- 100-1500A of 300-800A of amorphous silicon film 204 is preferably deposited by law. Although the membrane formation conditions in the LPCVD method are shown below, it is important to form membranes by LPCVD using the polysilane like a disilane, and it can raise the property of the polycrystal silicon film after crystallization by leaps and bounds here as compared with the plasma-CVD method by the glow discharge used for manufacture of the semiconductor device using conventional amorphous silicon. The membrane formation conditions in that case are Si2H6 typically. 100 - 500sccmHe 500sccm membrane formation temperature 430 degrees C - 500 degree-C membrane formation pressure 0.1 - 1Torr [0026] Furthermore, a substrate is transported to a reaction chamber 106, and about 500-1500A of oxidation silicon film 212 is deposited by the plasma-CVD method which uses TEOS as a raw material. This film functions as a protective coat of the silicon film. Membrane formation conditions are shown below.
TEOS/O2 =10 / 100sccmRF power Whenever [300 W-set board temperature] 350-degree-C membrane formation pressure 0.25 Torr, in this way, as shown in drawing 2 (A), nitriding aluminum or the blocking layer 202 of silicon nitride, the oxidation silicon film 203, the amorphous silicon semi-conductor film 204, and a protective coat 212 can be formed in succession on a glass substrate 201 at a multilayer. If there is not little equipment shown in this drawing 1 , it can make the value of C, N, and O especially in the silicon film three or less [5x1018cm -]. [since each chamber and the conveyance room with a robot arm are divided with the gate valve, respectively an impurity does not mix mutually between each chambers, and]
[0027] Next, a substrate is sent from a spare room 101 outside, and patterning for forming the island-like silicon field 204 is performed. And it is shown in drawing 2 (B) and the 500-1000A oxidation silicon film 205 is preferably formed 200-1500A in thickness like. This oxidation silicon film functions also as gate dielectric film. Therefore, sufficient cautions are required for the production. Here, TEOS was used as the raw material, and with oxygen, the substrate temperature of 350-600 degrees C, it is 300-450 degrees C preferably, and decomposed and deposited by RF plasma-CVD method. In the pressure ratio of TEOS and oxygen, 0.05 - 0.5torr and RF power set 1:1-1:3, and a pressure to 100-250W. From the carrying-in room 101, this process carries in a substrate, may carry out another actuation to having described above, and may perform it in a reaction chamber 106. Or 350-600 degrees C of substrate temperature may be preferably formed as 400-550 degrees C with a reduced pressure CVD method or an ordinary pressure CVD method with ozone gas by using TEOS as a raw material. It annealed at 400-600 degrees C by the ambient atmosphere of oxygen or ozone after membrane formation for 30 to 60 minutes.
[0028] When forming the oxidation silicon film 205 used as the above-mentioned gate dielectric film in a reaction chamber 106, it is effective to carry in a substrate to an annealing chamber 104 after the process termination, and to perform RAPITTO thermal annealing by infrared exposure in an N2 O ambient atmosphere. This has effectiveness in decreasing the interface state density of the oxidation silicon film 205 and the silicon field 204 extremely.
[0029] And as shown in drawing 2 (B), the KrF excimer laser 213 (the wavelength of 248nm ornm [308], 20ns of pulse width) was irradiated, and the silicon field 204 was crystallized. the energy density of laser -- 200 - 400 mJ/cm2 -- desirable -- 250 - 300 mJ/cm2 ** -- it carried out and the substrate was heated at 300-500 degrees C on the occasion of laser radiation. Thus, when the crystallinity of the formed silicon film 204 was

investigated by Raman-scattering spectroscopy, unlike the peak (521cm-1) of single crystal silicon, the comparatively broadcloth peak was observed by the 515cm-1 neighborhood, and it became clear that it had become a crystalline semi-conductor, for example, a polycrystal semi-conductor. Then, it annealed at 350 degrees C in hydrogen for 2 hours. The process of this crystallization may be performed by being based on heating.

[0030] Then, the aluminum film with a thickness of 2000A - 1 micrometer was formed with electron beam vacuum deposition, patterning of this was carried out and the gate electrode 206 was formed. To aluminum, a scandium (Sc) may be doped 0.15 to 0.2% of the weight. Next, the substrate was dipped in pH**7 and the ethylene glycol solution of 1 - 3% of tartaric acid, and platinum was anodized by considering as an anode plate in cathode and the gate electrode of this aluminum. Anodic oxidation raised the electrical potential difference with the fixed current to 220V at first, and in the condition, it was held for 1 hour and it ended it. In this example, the climbing speed of an electrical potential difference had the amount of suitable 2-5v/in the state of constant current. Thus, 1500-3500A in thickness and the 2000A anodic oxidation object 209 were formed. (Drawing 2 (C))

[0031] Moreover, what is necessary is just to use a tantalum instead of aluminum, in performing heat treatment in an elevated temperature.

[0032] then, the ion doping method (it is also called the plasma doping method) -- every -- the impurity (phosphorus) was poured in in self align by using the gate polar zone as a mask into the island-like silicon film of TFT. Phosphoretted hydrogen (PH3) was used as doping gas. The dose was set to 1-4x1015cm-2.

[0033] Furthermore, as shown in drawing 2 (D), the KrF excimer laser (the wavelength of 248nm or 308nm, 20ns of pulse width) 216 was irradiated, and the crystallinity of the part into which crystallinity deteriorated by installation of the above-mentioned impurity range was made to improve. the energy density of laser -- 150 - 400 mJ/cm2 -- desirable -- 200 - 250 mJ/cm2 it was . In this way, the N type impurity (phosphorus) fields 208 and 209 were formed. The sheet resistance of these fields was 200-800ohm/**. In this process, instead of using laser, it is made to go up for a short time to 1000-1200 degrees C (a silicon monitor's temperature) using a flash lamp, and the so-called RTP (rapid thermal process) which heats a sample may be used.

[0034] Then, again, using the equipment of drawing 1 , the reaction chamber 104 of the reactor of drawing 1 was again used for the whole surface as a layer insulation object 210, and 3000A (0.3 micrometers) formation of the oxidation silicon film was carried out 0.3 micrometers - 1 micrometer in thickness by using TEOS as a raw material here with the plasma-CVD method of this and oxygen, the reduced pressure CVD method with ozone, or the ordinary pressure CVD method. Substrate temperature was made into 250-450 degrees C, for example, 350 degrees C. After membrane formation, in order to obtain surface surface smoothness, this oxidation silicon film was ground mechanically. This process may perform isotropic dry etching using the reaction chamber prepared in the equipment of drawing 1 . Furthermore, by the spatter, the ITO coat was deposited, patterning of this was carried out, and it considered as the pixel electrode 211. (Drawing 2 (E))

[0035] If it writes and carries out, a thin film integrated circuit can be made to one substrate side of the electro-optic device of drawing 2 . Of course, a circumference circuit may be formed on the same substrate at the circuit and coincidence which are shown in this drawing. And the layer insulation object 210 was etched, as shown in drawing 2 (E), the contact hole was formed in the source/drain of TFT, the wiring 212 and 213 of chromium or titanium nitride was formed, and wiring 213 was connected to the pixel electrode 211. in addition, in this case, it is **** about the source / drain field (island-like silicon) -- it may carry out and a contact hole may be formed. in this case, it is **** about island-like silicon among contact holes -- the area carried out was 30 - 70%. In this case, contact is formed also not only in the top face of the source/drain but in a side face. Hereafter, such contact is called top side contact. In the conventional structure, although even the substrate was etched into the oxidization silicon film of the substrate of parts other than island-like silicon, and a pan by the etching process of a layer insulation object when it was going to form top side contact, the alumimium nitride film or a silicon nitride film 202 serves as an etching stopper, and etching stops at this example here.

[0036] although magnitude of a contact hole needed to be made smaller than the source/drain in the usual case -- top side contact -- setting -- reverse -- the magnitude of an island -- that of a contact hole -- small -- it can do -- as a result -- an island -- detailed -- it can do-izing. Moreover, since the KONTAKU hole was enlarged conversely, mass-production nature and dependability were able to be raised.

[0037] Finally, it annealed at 300-400 degrees C in hydrogen for 0.1 to 2 hours, and hydrogenation of silicon was completed. Thus, the thin film integrated circuit which has TFT was completed. And it considered as the active matrix liquid crystal display of the MONOSHI rucksack mold which was made to arrange TFT of a large number

produced to coincidence in the shape of a matrix, and also formed the circumference circuit on the same substrate.

[0038] [Example 3] The example which produces the thin film integrated circuit which has at least one TFT using the multiple-purpose membrane formation equipment shown in drawing 1 is shown in drawing 3 . First, the multiple-purpose membrane formation equipment used in this example is explained. In this example, 101 was made into the spare room, in order to perform carrying-in taking out of a substrate. moreover — the processing room which makes 106 the processing room which heats, makes 103 the processing room which forms a silicon nitride film by the plasma-CVD method, uses TEOS as a raw material for 104, and forms the oxidation silicon film by the plasma-CVD method — carrying out — 105 — LPCVD — it considers as the processing room which forms the amorphous silicon film by law. Moreover, it considered as the processing room which forms the polycrystal silicon film which doped P for 102 with a reduced pressure heat CVD method. Moreover, the gas installation means for introducing the exhaust air means for changing each processing room into a reduced pressure condition and the gas needed further is formed in each processing room.

[0039] A making process is shown below. First, the heat-resistant high crystallization glass plate (a 4 inch angle, a 5 inch angle, or 5x6 inch angle) 201 represented by N0 glass as a substrate is carried in to a spare room 101, and vacuum suction is carried out enough. As for this vacuum suction, it is desirable to carry out until it becomes the almost same pressure as the conveyance room 107 enough carried out in vacuum suction. And a gate valve 110 is opened and the substrate in a spare room 101 is transported to the conveyance room 107 by the robot arm 108. In drawing 1 , the substrate 201 in drawing 3 is shown as 109. In addition, it is called a substrate also including the film currently formed on it below. And the gate valve 112 between the reaction chambers 103 where vacuum suction was similarly mostly carried out to the same pressure is opened, and a substrate is carried in. A gate valve 112 is shut after substrate carrying in, and it sets in this reaction chamber 103, and is a silicon nitride film 200 by the plasma-CVD method The substrate temperature of 350 degrees C, 0.1Torr, and SiH4 NH3 Membranes are formed in a mixed ambient atmosphere. This silicon nitride film is for preventing diffusion of the alkali from a substrate.

[0040] And vacuum suction of the reaction chamber 103 is carried out, and a substrate is transported to the conveyance room 107 where vacuum suction was carried out again by the robot arm 108. And a substrate is conveyed to the reaction chamber 106 where vacuum suction was similarly carried out. In this reaction chamber 106, the oxidation silicon film 203 is formed by the plasma-CVD method which used TEOS as the raw material. Membrane formation conditions are shown below.

TEOS/O2 =10 / 100sccmRF power Whenever [350 W-set board temperature] 400-degree-C membrane formation pressure 0.25Torr [0041] Moreover, it sets for the above-mentioned reaction and is C two F6. It adds and is SiOFx. The film shown may be formed.

[0042] This oxidation silicon film is formed as a substrate oxide film 203 by 2000-50A in thickness in the field which forms TFT.

[0043] And a substrate is again conveyed in the conveyance room 107, and then a substrate is carried in to a reaction chamber 105. All the things that a conveyance room and each processing room make open and close a gate valve in the case of migration of these substrates after vacuum suction is carried out to the same degree of vacuum (the same reduced pressure condition) are common.

[0044] a reaction chamber 105 — LPCVD — 200-2000A of 300-800A of amorphous silicon film 204 is preferably deposited by law. The membrane formation conditions in the LPCVD method are shown below.

Si2H6 100sccmHe Whenever [200sccm stoving temperature] 500 degrees C - 570 degree-C membrane formation pressure 0.3Torr growth rate A part for 50A - 500A/[0045] Here, the polycrystal silicon film with the sufficient property of having the mean particle diameter of 250A - 8000A in a subsequent heat crystallization process can be obtained by it being important to use the polysilane like a disilane and forming membranes on condition that the above using these.

[0046] Then, in order to take out, the substrate which processing ended is again brought together in a spare room 101, and is taken out to the exterior of equipment.

[0047] This is for carrying out patterning of the amorphous silicon film 204 to the shape of an island, and crystallizing after an appropriate time. This is because it is more efficient to consider as another equipment in order for the time amount which these processes' not being processes under reduced pressure and these processes take to raise the operating ratio of equipment as compared with the time amount which other processes take, since it is extraordinarily long.

[0048] Patterning of the amorphous silicon film 204 performs patterning in the shape of [predetermined] an

island using well-known photolithography.
[0049] Heat crystallization is performed by heating from 8 hours at 550 degrees C - 600 degrees C in nitrogen-gas-atmosphere mind for 56 hours. Thus, the crystal of the above big particle size can be obtained by crystallizing at low temperature comparatively.
[0050] Then, in 800 degrees C - 850 degrees C, heat annealing is performed on the highest possible temperature and a concrete target within the limits of the heat-resistant temperature of N0 glass. This process enables it to raise the crystallinity in each crystal grain. Moreover, this process may be performed in an oxidizing atmosphere, for example, dry oxygen, and the thermal oxidation film may be formed in coincidence. When using this thermal oxidation film as gate dielectric film, it is appropriate for that thickness to consider as 500A - 2000A.
[0051] Thus, the substrate which finished crystal growth is again thrown in in equipment from a spare room 101.
[0052] The substrate thrown in from the spare room 101 transports a substrate to a reaction chamber 104 further if needed, by the plasma-CVD method which uses TEOS as a raw material, is shown in drawing 3 (B) and forms the 500-1000A oxidation silicon film 205 preferably 200-1500A in thickness like. Here, TEOS was used as the raw material, and with oxygen, the substrate temperature of 350-600 degrees C, it is 300-450 degrees C preferably, and decomposed and deposited by RF plasma-CVD method. In the pressure ratio of TEOS and oxygen, 0.05 - 0.5torr and RF power set 1:1-1:3, and a pressure to 100-250W.
[0053] This process may form preferably 350-600 degrees C of substrate temperature as 400-550 degrees C with a reduced pressure CVD method or an ordinary pressure CVD method with ozone gas by using TEOS as a raw material.
[0054] Moreover, it annealed at 400-600 degrees C by the ambient atmosphere of oxygen or ozone after membrane formation for 30 to 60 minutes.
[0055] When membrane formation of the above-mentioned oxidation silicon film 205 performs elevated-temperature annealing after heat crystallization in an oxidizing atmosphere and it uses the thermal oxidation film as gate dielectric film, it cannot be overemphasized that this process becomes unnecessary.
[0056] In this way, as shown in drawing 3 (B), the blocking layer 202 of silicon nitride, the oxidation silicon film 203, the crystalline silicon semi-conductor film 204 by which patterning was carried out to the shape of an island, and the oxidation silicon film 205 can be formed on a glass substrate 201 at a multilayer. If there is not little equipment shown in this drawing 1 , it can make the value of C, N, and O especially in the silicon film three or less [5x1018cm -]. [since each chamber and the conveyance room with a robot arm are divided with the gate valve, respectively an impurity does not mix mutually between each chambers, and]
[0057] When forming the oxidation silicon film 205 used as the above-mentioned gate dielectric film in a reaction chamber 104, it is effective to carry in a substrate to an annealing chamber 106 after the process termination, and to perform RAPITTO thermal annealing by infrared exposure in an N2 O ambient atmosphere. This has effectiveness in decreasing the interface state density of the oxidation silicon film 205 and the silicon field 204 extremely.
[0058] Next, the polycrystal silicon film which doped P used as a gate electrode is formed with the reduced pressure heat CVD on the above-mentioned gate dielectric film at the thickness of 1000A - 4000A.
[0059] Especially the field side to [to the above-mentioned process (i.e., from a substrate)] a silicon semi-conductor layer, gate dielectric film, and a gate electrode is sensitive to interface state density etc., and it is the main parts which determine the property of a device, and without so being exposed to atmospheric air, it is desirable to form membranes continuously and it of it becomes possible by the configuration of this invention.
[0060] From the equipment of this invention, the following processes are taken out outside and performed.
[0061] First, dry etching performs patterning for the polycrystal silicon film which doped P that the gate electrode 217 should be formed. (Drawing 3 (C))
[0062] then, the ion doping method (it is also called the plasma doping method) -- every -- an impurity (phosphorus) is poured in in self align by using the gate electrode 217 as a mask into the island-like silicon film of TFT. Phosphoretted hydrogen (PH3) was used as doping gas. The dose was set to 1-4x1015cm-2.
[0063] Next, after heating 600 degrees C of substrates in nitrogen-gas-atmosphere mind for 12 hours and activating a dopant, further, in a hydrogen ambient atmosphere, by 400 degrees C, it heat-treats for 1 hour, a hydrogen treating is performed, and the defective level consistency of a semi-conductor layer is decreased.
[0064] then, other equipments -- or an interlayer insulation film 210 is again formed in the whole surface using the equipment of drawing 1 . When the equipment of drawing 1 was used, 3000A (0.3 micrometers) formation of the oxidation silicon film was carried out 0.3 micrometers - 1 micrometer in thickness by using TEOS as a raw material here with the plasma-CVD method of this and oxygen, the reduced pressure CVD method with ozone,

or the ordinary pressure CVD method, using the reaction chamber 104 of the reactor of drawing 1 again. Substrate temperature was made into 250-450 degrees C, for example, 350 degrees C. After membrane formation, in order to obtain surface surface smoothness, this oxidation silicon film was ground mechanically. This process may perform isotropic dry etching using the reaction chamber prepared in the equipment of drawing 1 . Furthermore, by the spatter, the ITO coat was deposited, patterning of this was carried out, and it considered as the pixel electrode 211. (Drawing 3 (E))

[0065] If it writes and carries out, a thin film integrated circuit can be made to one substrate side of an electro-optic device. Of course, a circumference circuit may be formed on the same substrate at the circuit and coincidence which are shown in this drawing. And the layer insulation object 210 was etched, as shown in drawing F (E), the contact hole was formed in the source/drain of TFT, the wiring 212 and 213 of chromium or titanium nitride was formed, and wiring 213 was connected to the pixel electrode 211. in addition, in this case, it is **** about the source / drain field (island-like silicon) -- it may carry out and a contact hole may be formed. in this case, it is **** about island-like silicon among contact holes -- the area carried out was 30 - 70%. In this case, contact is formed also not only in the top face of the source/drain but in a side face. Hereafter, such contact is called top side contact. In the conventional structure, although even the substrate was etched into the oxidization silicon film of the substrate of parts other than island-like silicon, and a pan by the etching process of a layer insulation object when it was going to form top side contact, a silicon nitride film 200 serves as an etching stopper, and etching stops at this example here.

[0066] In the usual case, although magnitude of a contact hole needed to be made smaller than the source/drain, in top side contact, it can make magnitude of an island smaller than a contact hole conversely, and detailed-ization of an island can do it as a result. Moreover, since the KONTAKU hole was enlarged conversely, mass-production nature and dependability were able to be raised.

[0067] Thus, the thin film integrated circuit which has TFT was completed. And it considered as the active matrix liquid crystal display of the MONOSHI rucksack mold which was made to arrange TFT of a large number produced to coincidence in the shape of a matrix, and also formed the circumference circuit on the same substrate.

[0068] In addition, when a substrate is used as a quartz substrate in the above-mentioned example, the oxidation silicon film of a substrate can be omitted and may also omit the oxidation silicon film of a substrate depending on the case. Moreover, since the thermal resistance of a substrate is high, it is possible to raise the temperature of heat annealing after heat crystallization or the process of thermal oxidation to about 1000 degrees C, and it is possible to obtain the crystalline good silicon film in that case further.

[0069]

[Effect] By adopting the configuration of this invention, a process can be managed succeeding the time of producing the semiconductor device which consists of polycrystal silicon on a substrate, and improvement in productivity and improvement in dependability can be achieved to coincidence.

[0070] As explained above, one equipment can perform the process of drawing 2 (A), formation of gate dielectric film, RTP down stream processing, and the making process and almost all the processes of an interlayer insulation film by using the multiple-purpose CVD system of the multi chamber method of drawing 1 . And these processes can be controlled by the microcomputer and can raise productive efficiency and cost performance. especially this invention equipment was shown in drawing 2 -- as -- crystallinity -- applying to the MONOSHI rucksack mold thin film integrated circuit adapting TFT or this can acquire remarkable effectiveness.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Industrial Application] This invention relates to the equipment which forms in a substrate top or a substrate front face the semiconductor device which consists of polycrystal silicon. It is related with the equipment which can perform a process with the need put especially to the open air of being continuously carried out without ******. Moreover, it is related with the multiple-purpose substrate processor which can be used for production of a thin film integrated circuit.

[Translation done.]

PRIOR ART

[Description of the Prior Art] The integrated circuit using a semi-conductor substrate or a glass substrate is known. IC and LSI are known as the former and the liquid crystal display of an active-matrix mold is known as the latter. In order to form such an integrated circuit, it is necessary to perform various processes continuously. For example, if it is the case where an insulated-gate mold electric field effect semiconductor device is formed, to form continuously is desired, without taking out outside the semiconductor region in which a channel is formed, and the gate dielectric film formed in contact with it. Moreover, it is the industry top need to perform various processes continuously efficiently.
[0003] Although it was desirable to these manufactures to perform a membrane formation process continuously within one equipment, the equipment with which only the manufacturing installation aiming at the manufacturing installation aiming at the semiconductor device with which the conventional manufacturing installation used amorphous silicon, or the semiconductor device using single crystal silicon existed but with which it was suitable for the semiconductor device using polycrystal silicon, and the manufacture approach using it were not established.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect] By adopting the configuration of this invention, a process can be managed succeeding the time of producing the semiconductor device which consists of polycrystal silicon on a substrate, and improvement in productivity and improvement in dependability can be achieved to coincidence.
[0070] As explained above, one equipment can perform the process of drawing 2 (A), formation of gate dielectric film, RTP down stream processing, and the making process and almost all the processes of an interlayer insulation film by using the multiple-purpose CVD system of the multi chamber method of drawing 1 . And these processes can be controlled by the microcomputer and can raise productive efficiency and cost performance. especially this invention equipment was shown in drawing 2 -- as -- crystallinity -- applying to the MONOSHI rucksack mold thin film integrated circuit adapting TFT or this can acquire remarkable effectiveness.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] This invention aims at offering the substrate processor which can process continuously the various processes needed for production of a semiconductor device which used polycrystal silicon with one equipment and which can be used for multiple purposes. In order to produce the semi-conductor especially using polycrystal silicon with a sufficient property, it is an indispensable configuration in said substrate processor that it is possible to form the insulator layer which needs to be prepared in contact with either [its] both to have the means forming of the silicon film by the reduced pressure heat CVD which used polysilane, or its upper and lower sides by plasma CVD.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

MEANS

[The means for heating a technical problem] In order to produce the semiconductor device which has the barrier layer which consists of polycrystal silicon with a sufficient property, the multiple-purpose substrate processor of this invention Have the processing room in which two or more reduced pressure is possible, and said two or more processing rooms are connected through the community room which can be decompressed. It has a means for conveying a substrate between each processing room in said community room. Membrane formation of the silicon film by the reduced pressure heat CVD is possible for at least one of said two or more processing rooms, and membrane formation of the oxidation silicon film by plasma CVD or a silicon nitride film is possible for at least one of said two or more processing rooms, Or have the processing room in which two or more reduced pressure is possible, and said two or more processing rooms are connected through the community room which can be decompressed. It has a means for conveying a substrate between each processing room in said community room. Membrane formation of the silicon film by the reduced pressure heat CVD is possible for at least one of said two or more processing rooms, and membrane formation of the oxidation silicon film by plasma CVD is possible for at least one of said two or more processing rooms. At least one of said two or more processing rooms is characterized [the / biggest] by membrane formation of the silicon nitride film by plasma CVD being possible.
[0006] In order to produce the semiconductor device which has the barrier layer which consists of polycrystal silicon with a sufficient property, moreover, the approach of the multiple-purpose substrate processor of this invention of operation In the condition of having been held at the same pressure, the substrate held at any one processing room is transported to a community room, Or the thing for which the substrate held at the community room is transported to any one processing room, And the thing for which the silicon film is formed with the reduced pressure heat CVD in at least one of said processing rooms, And the thing for which plasma CVD performs membrane formation of the oxidation silicon film, or membrane formation of a silicon nitride film in at least one of said processing rooms Or the thing for which the substrate held at any one processing room is transported to a community room in the condition of having been held at the same pressure, Or the thing for which the substrate held at the community room is transported to any one processing room, And the thing for which the silicon film is formed with the reduced pressure heat CVD in at least one of said processing rooms, And it is characterized [the] especially by the thing for which a silicon nitride film is formed by plasma CVD in at least one of forming the oxidation silicon film by plasma CVD in at least one of said processing rooms, and said processing rooms.
[0007] If the need of taking the above configurations is described briefly, the manufacture process of a semiconductor device of having used amorphous silicon will have been conventionally used for manufacture of the semiconductor device using polycrystal silicon chiefly. The plasma CVD which used glow discharge is used for membrane formation of the silicon film in that case. The silicon film produced by making it the appearance contains a lot of hydrogen, and a membranous condition changes a lot with emission of the hydrogen at the time of making it crystallize etc. It became clear that it is difficult to obtain the semiconductor device which consists a configuration like continuation membrane formation which had many processing rooms with much trouble of polycrystal silicon which has very sufficient property as a result of the experiment. In order to solve this trouble, it turned out using LPCVD that it is effective to use the polysilane like a disilane as material gas.
[0008] However, in an existing manufacturing installation and an existing manufacture process, since it was once exposed into atmospheric air even if it is the case where LPCVD is used, it was difficult to obtain the semiconductor device which consists of polycrystal silicon which cannot form an interface with a sufficient property but has too sufficient property. So, in order to realize junction of the most important, beautiful

interface, it is forming membrane formation of the silicon film by LPCVD, and the insulator layer which needs to be prepared in contact with both the upper and lower sides or one of these, without opening to atmospheric air continuously, and it became clear by experiment of artificers for the fast improvement in a property to be possible. As the membrane formation approach of this insulator layer, the conclusion that the approach by plasma CVD was the best was reached in consideration of the property, the throughput, etc. from artificers' experimental result.

[0009] The concrete example of this invention is shown in drawing 1 . The equipment shown in drawing 1 can be used for multiple purposes, and can be combined by the number which needs the processing room which performs membrane formation to need and annealing treatment. A glass substrate, a silicon substrate, other insulating substrates, and a semi-conductor substrate can be used as a substrate processed with the equipment shown in drawing 1 . That is, if it is the substrate which has an insulating front face, it can use. For example, if it is electro-optic devices, such as a liquid crystal display of a active-matrix mold, and image sensors, it is common to use a cheap glass substrate.

[0010] For example, 107 is made into the conveyance room of the substrate which is a community room, 101 and 102 are made into a spare room among the processing rooms which perform various processings of a substrate, one side is used for carrying in of a substrate, and other one side is used for taking out of a substrate. Moreover, the configuration that 103 considers as the plasma-CVD equipment for forming an insulator layer, uses 104 as the reduced pressure heat CVD system for forming amorphous silicon, uses 105 as the heating furnace for forming the thermal oxidation film, and considers as the annealing furnace for performing annealing according 106 to an optical exposure can be taken. In addition, a spare room can also be called processing room for the purpose of having the function to perform carrying in and taking out of a substrate.

[0011] Such a combination can be performed to arbitration. As an element which can do these combination, plasma CVD, the reduced pressure heat CVD (in this specification, it abbreviates to LPCVD below), Light CVD, microwave CVD, a heating furnace, the annealing furnace by optical exposure, sputtering, plasma annealing, and plasma etching can be mentioned.

[Translation done.]

* NOTICES *

EXAMPLE

[Example]
[Example 1] The configuration of this example is shown in drawing 1 . In this example, 101 and 102 are spare rooms and it has the function to take a substrate in and out. These chambers have the function to hold the cassette by which two or more substrates were stored. Moreover, naturally in the introductory means of inert gas, the introductory means of cleaning gas, and the pan, it has the flueing means.
[0013] 103-106 are processing rooms, 103 and 106 are plasma-CVD equipment, and 104 is a temperature control chamber. A temperature control chamber has the function to heat a substrate to predetermined temperature, and in advance of membrane formation by other chambers, it is used in order to heat the substrate beforehand. The specification of each processing room is shown in the following table 1.
[0014]
[Table 1]

	106	105	104	103
処理内容	PCVD	予備加熱 RTP	PCVD LPCVD	PCVD
RF電源	13.56MHz 500 W	———	13.56MHz 500 W	13.56MHz 500 W
電　極	平行平板	平行平板	平行平板	平行平板
プロセスガス	N_2, SiH_4, NH_3 $Al(CH_3)_3$	N_2O, N_2, NH_3, O_2	N_2, SiH_4, H_2 Si_2H_6, Si_3H_8	N_2, TEOS, O_2 C_2F_6
クリーニングガス	NF_3 +N_2	———	NF_3 +N_2	NF_3 +N_2
基板加熱温度	450℃	450℃	550℃	600℃
膜	Si_2H_4 AlN	———	Si	SiO_2 SiF_x
排気設備	到達圧力 5×10^{-2}Torr	到達圧力 5×10^{-2}Torr	到達圧力 5×10^{-5}Torr	到達圧力 5×10^{-2}Torr

尚、基板サイズとしては、4インチ角、5インチ角、5×6インチ角を利用することができる。

[0015] 107 is the conveyance room of a substrate and a substrate has between each chamber conveyed by the robot arm 108. The robot arm 108 has the function for which takes out one substrate (shown by 109) at a time from a spare room 101 or 102, and it is moved to the reaction chamber to need. Naturally a substrate can be moved between each processing room. Moreover, the exhaust air means is formed also in this conveyance room, and it can be made the degree of vacuum to need.
[0016] Migration of the substrate between each chamber is performed by [as being the following]. For example, the substrate held in a spare room 101 is processed at the processing rooms 103 and 104, and the case where it carries in to a spare room 102 is considered. In this case, first, the (1) spare room 101 and the conveyance room 107 are made into the same reduced pressure condition (a high vacuum condition is desirable), a gate valve 110 is opened in that condition, and a substrate 109 is taken out in a conveyance room by the robot arm 108. A gate

valve 110 is shut after that.
(2) Make the conveyance room 107 and the processing room 103 into the same reduced pressure condition, open a gate valve 112 in the condition, and carry in to a process room the substrate 109 held at the robot arm 108. A gate valve 112 is shut after that.
(3) A predetermined process is performed at the processing room 103.
(4) Make the degree of vacuum of the processing room 103 into the same reduced pressure condition as the conveyance room 107 after process ending at the processing room 103, open a gate valve 112 after that, and take out a substrate in the conveyance room 107 by the robot arm 108. And a gate valve 112 is shut.
(5) Make the conveyance room 107 and the processing room 104 into the same reduced pressure condition, open a gate valve 113 in the condition, and carry in to the processing room 104 the substrate held at the robot arm 108. A gate valve is shut after that.
(6) A predetermined process is performed at the processing room 104.
(7) Make the degree of vacuum of the processing room 104 into the same reduced pressure condition as the conveyance room 107 after process ending at the processing room 104, open a gate valve 113 after that, and take out a substrate in the conveyance room 107 by the robot arm 108. And a gate valve 113 is shut.
(8) Make the conveyance room 107 and a spare room 102 into the same reduced pressure condition, open a gate valve 111 in the condition, by the robot arm 108, carry in a substrate to a spare room 102 and shut a gate valve 111 after that.
[0017] Processing beyond 2 times or it can be performed continuously, without putting one substrate to the open air as mentioned above. It is useful that not only membrane formation but annealing etc. can be performed as these processings.
[0018] The above (1) By repeating the process of - (8), two or more substrates held at the cartridge carried in to the spare room 101 can be continuously processed from a degree to a degree. And the substrate which processing ended will be held automatically at the cartridge of a spare room 102. Moreover, in the above-mentioned membrane formation process, down stream processing which continued while cleaning can be performed, without stopping the whole actuation by cleaning the processing room 104, and cleaning the processing room 103 conversely, while the processing room 104 works, while the processing room 103 works. As such cleaning, it is NF3. The plasma cleaning in the chamber to depend can be mentioned.
[0019] [Example 2] The example which produces the thin film integrated circuit which has at least one TFT which makes polycrystal silicon a barrier layer using the multiple-purpose membrane formation equipment shown in drawing 1 is shown in drawing 2 . First, the multiple-purpose membrane formation equipment used in this example is explained. In this example, 101 and 106 were made into the spare room, in order to perform carrying-in taking out of a substrate. 106 were especially carried out for 101 to substrate taking out for substrate carrying in here. Moreover, the RAPITTO thermal annealing process according 104 to the short-time exposure of infrared light (it is called RTA or RTP), Or it considers as the processing room which forms the film (nitriding aluminum oxide is called alumimium nitride below) or silicon nitride film which considers as the processing room which performs preheating and uses alumimium nitride as a principal component for 103 by the plasma-CVD method. the processing room which uses TEOS as a raw material for 104, and forms the oxidation silicon film by the plasma-CVD method -- carrying out -- 105 -- LPCVD -- it considers as the processing room which forms the amorphous silicon film by law. Moreover, the gas installation means for introducing the exhaust air means for changing each processing room into a reduced pressure condition and the gas needed further is formed in each processing room.
[0020] A making process is shown below. First, the glass substrate (a 4 inch angle, a 5 inch angle, or 5x6 inch angle) 201 of Corning 7059 grade is carried in to a spare room 101 as a substrate, and vacuum suction is carried out enough. As for this vacuum suction, it is desirable to carry out until it becomes the almost same pressure as the conveyance room 107 enough carried out in vacuum suction. And a gate valve 110 is opened and the substrate in a spare room 101 is transported to the conveyance room 107 by the robot arm 108. In drawing 1 , the substrate 201 in drawing 2 is shown as 109. In addition, it is called a substrate also including the film currently formed on it below. And the gate valve 112 between the reaction chambers 103 where vacuum suction was similarly mostly carried out to the same pressure is opened, and a substrate is carried in. A gate valve 112 is shut after substrate carrying in, and the alumimium nitride film 202 with a thickness of 2000-5000A is formed by the plasma-CVD method in this reaction chamber 103. Membrane formation is aluminum (C four H9)3. Or aluminum3 (CH3) N2 It carries out by using. Moreover, minute amount addition of the N2 O may be carried out, and thermal-expansion distortion may be made to ease.

[0021] After membrane formation of the alumimium nitride film 202 carries out vacuum suction of the reaction chamber 103 to the same degree of vacuum as the conveyance room 107. And a gate valve 112 is opened and a substrate is transported for a substrate to a conveyance room by the robot arm 108. Next, a substrate is carried in to the annealing chamber 104 where vacuum suction was similarly carried out. In this annealing chamber 104, RAPITTO thermal annealing (RTA) by infrared exposure is performed. This annealing is performed in the ambient atmosphere of nitrogen, ammonia (NH3), or nitrous oxide (N2 O), and heats the alumimium nitride film quickly for a short time. By this annealing, the alumimium nitride film becomes transparent and its insulation and thermal conductivity of that improve. Moreover, in order to prevent the penetration to the semi-conductor of impurities, such as NATORYUMU from a glass substrate, a silicon nitride film may be formed. In this case, it is a silicon nitride film by the plasma-CVD method The substrate temperature of 350 degrees C, 0.1Torr, and SiH4 NH3 Membranes are formed in a mixed ambient atmosphere.
[0022] And vacuum suction of the reaction chamber 104 is carried out, and a substrate is transported to the conveyance room 107 where vacuum suction was carried out again by the robot arm 108. And a substrate is conveyed to the reaction chamber 106 where vacuum suction was similarly carried out. In this reaction chamber 106, the oxidation silicon film 203 is formed by the plasma-CVD method which used TEOS as the raw material. Membrane formation conditions are shown below.
TEOS/O2 =10 / 100sccmRF Power Whenever [350 W-set board temperature] 400-degree-C membrane formation pressure 0.25 Torr, it sets for the above-mentioned reaction and is C two F6 again. It adds and is SiOFx. The film shown may be formed.
[0023] This oxidation silicon film is formed as a substrate oxide film 203 by 2000-50A in thickness in the field which forms TFT. The oxidation silicon film 203 formed in this reaction chamber 106 may be conveyed to an annealing chamber 104, and RAPITTO thermal annealing may be performed.
[0024] And a substrate is again conveyed in the conveyance room 107, and then a substrate is carried in to a reaction chamber 105. All the things that a conveyance room and each processing room make open and close a gate valve in the case of migration of these substrates after vacuum suction is carried out to the same degree of vacuum (the same reduced pressure condition) are common.
[0025] a reaction chamber 105 -- LPCVD -- 100-1500A of 300-800A of amorphous silicon film 204 is preferably deposited by law. Although the membrane formation conditions in the LPCVD method are shown below, it is important to form membranes by LPCVD using the polysilane like a disilane, and it can raise the property of the polycrystal silicon film after crystallization by leaps and bounds here as compared with the plasma-CVD method by the glow discharge used for manufacture of the semiconductor device using conventional amorphous silicon. The membrane formation conditions in that case are Si2H6 typically. 100 - 500sccmHe 500sccm membrane formation temperature 430 degrees C - 500 degree-C membrane formation pressure 0.1 - 1Torr [0026] Furthermore, a substrate is transported to a reaction chamber 106, and about 500-1500A of oxidation silicon film 212 is deposited by the plasma-CVD method which uses TEOS as a raw material. This film functions as a protective coat of the silicon film. Membrane formation conditions are shown below.
TEOS/O2 =10 / 100sccmRF Power Whenever [300 W-set board temperature] 350-degree-C membrane formation pressure 0.25 Torr, in this way, as shown in drawing 2 (A), nitriding aluminum or the blocking layer 202 of silicon nitride, the oxidation silicon film 203, the amorphous silicon semi-conductor film 204, and a protective coat 212 can be formed in succession on a glass substrate 201 at a multilayer. If there is not little equipment shown in this drawing 1 , it can make the value of C, N, and O especially in the silicon film three or less [5x1018cm -]. [since each chamber and the conveyance room with a robot arm are divided with the gate valve, respectively an impurity does not mix mutually between each chambers, and]
[0027] Next, a substrate is sent from a spare room 101 outside, and patterning for forming the island-like silicon field 204 is performed. And it is shown in drawing 2 (B) and the 500-1000A oxidation silicon film 205 is preferably formed 200-1500A in thickness like. This oxidation silicon film functions also as gate dielectric film. Therefore, sufficient cautions are required for the production. Here, TEOS was used as the raw material, and with oxygen, the substrate temperature of 350-600 degrees C, it is 300-450 degrees C preferably, and decomposed and deposited by RF plasma-CVD method. In the pressure ratio of TEOS and oxygen, 0.05 - 0.5torr and RF Power set 1:1-1:3, and a pressure to 100-250W. From the carrying-in room 101, this process carries in a substrate, may carry out another actuation to having described above, and may perform it in a reaction chamber 106. Or - 350-600 degrees C of substrate temperature may be preferably formed as 400-550 degrees C with a reduced pressure CVD method or an ordinary pressure CVD method with ozone gas by using TEOS as a raw material. It annealed at 400-600 degrees C by the ambient atmosphere of oxygen or ozone after membrane formation for 30

to 60 minutes.
[0028] When forming the oxidation silicon film 205 used as the above-mentioned gate dielectric film in a reaction chamber 106, it is effective to carry in a substrate to an annealing chamber 104 after the process termination, and to perform RAPITTO thermal annealing by infrared exposure in an N2 O ambient atmosphere. This has effectiveness in decreasing the interface state density of the oxidation silicon film 205 and the silicon field 204 extremely.
[0029] And as shown in drawing 2 (B), the KrF excimer laser 213 (the wavelength of 248nm ornm [308], 20ns of pulse width) was irradiated, and the silicon field 204 was crystallized. the energy density of laser -- 200 - 400 mJ/cm2 -- desirable -- 250 - 300 mJ/cm2 ** -- it carried out and the substrate was heated at 300-500 degrees C on the occasion of laser radiation. Thus, when the crystallinity of the formed silicon film 204 was investigated by Raman-scattering spectroscopy, unlike the peak (521cm-1) of single crystal silicon, the comparatively broadcloth peak was observed by the 515cm-1 neighborhood, and it became clear that it had become a crystalline semi-conductor, for example, a polycrystal semi-conductor. Then, it annealed at 350 degrees C in hydrogen for 2 hours. The process of this crystallization may be performed by being based on heating.
[0030] Then, the aluminum film with a thickness of 2000A - 1 micrometer was formed with electron beam vacuum deposition, patterning of this was carried out and the gate electrode 206 was formed. To aluminum, a scandium (Sc) may be doped 0.15 to 0.2% of the weight. Next, the substrate was dipped in pH**7 and the ethylene glycol solution of 1 - 3% of tartaric acid, and platinum was anodized by considering as an anode plate in cathode and the gate electrode of this aluminum. Anodic oxidation raised the electrical potential difference with the fixed current to 220V at first, and in the condition, it was held for 1 hour and it ended it. In this example, the climbing speed of an electrical potential difference had the amount of suitable 2-5v/in the state of constant current. Thus, 1500-3500A in thickness and the 2000A anodic oxidation object 209 were formed. (Drawing 2 (C))
[0031] Moreover, what is necessary is just to use a tantalum instead of aluminum, in performing heat treatment in an elevated temperature.
[0032] then, the ion doping method (it is also called the plasma doping method) -- every -- the impurity (phosphorus) was poured in in self align by using the gate polar zone as a mask into the island-like silicon film of TFT. Phosphoretted hydrogen (PH3) was used as doping gas. The dose was set to 1-4x1015cm-2.
[0033] Furthermore, as shown in drawing 2 (D), the KrF excimer laser (the wavelength of 248nm or 308nm, 20ns of pulse width) 216 was irradiated, and the crystallinity of the part into which crystallinity deteriorated by installation of the above-mentioned impurity range was made to improve. the energy density of laser -- 150 - 400 mJ/cm2 -- desirable -- 200 - 250 mJ/cm2 it was . In this way, the N type impurity (phosphorus) fields 208 and 209 were formed. The sheet resistance of these fields was 200-800ohm/**. In this process, instead of using laser, it is made to go up for a short time to 1000-1200 degrees C (a silicon monitor's temperature) using a flash lamp, and the so-called RTP (rapid thermal process) which heats a sample may be used.
[0034] Then, again, using the equipment of drawing 1 , the reaction chamber 104 of the reactor of drawing 1 was again used for the whole surface as a layer insulation object 210, and 3000A (0.3 micrometers) formation of the oxidation silicon film was carried out 0.3 micrometers - 1 micrometer in thickness by using TEOS as a raw material here with the plasma-CVD method of this and oxygen, the reduced pressure CVD method with ozone, or the ordinary pressure CVD method. Substrate temperature was made into 250-450 degrees C, for example, 350 degrees C. After membrane formation, in order to obtain surface surface smoothness, this oxidation silicon film was ground mechanically. This process may perform isotropic dry etching using the reaction chamber prepared in the equipment of drawing 1 . Furthermore, by the spatter, the ITO coat was deposited, patterning of this was carried out, and it considered as the pixel electrode 211. (Drawing 2 (E))
[0035] If it writes and carries out, a thin film integrated circuit can be made to one substrate side of the electro-optic device of drawing 2 . Of course, a circumference circuit may be formed on the same substrate at the circuit and coincidence which are shown in this drawing. And the layer insulation object 210 was etched, as shown in drawing 2 (E), the contact hole was formed in the source/drain of TFT, the wiring 212 and 213 of chromium or titanium nitride was formed, and wiring 213 was connected to the pixel electrode 211. in addition, in this case, it is **** about the source / drain field (island-like silicon) -- it may carry out and a contact hole may be formed. in this case, it is **** about island-like silicon among contact holes -- the area carried out was 30 - 70%. In this case, contact is formed also not only in the top face of the source/drain but in a side face. Hereafter, such contact is called top side contact. In the conventional structure, although even the substrate

was etched into the oxidization silicon film of the substrate of parts other than island-like silicon, and a pan by the etching process of a layer insulation object when it was going to form top side contact, the alumimium nitride film or a silicon nitride film 202 serves as an etching stopper, and etching stops at this example here.
[0036] although magnitude of a contact hole needed to be made smaller than the source/drain in the usual case -- top side contact -- setting -- reverse -- the magnitude of an island -- that of a contact hole -- small -- it can do -- as a result -- an island -- detailed -- it can do-izing. Moreover, since the KONTAKU hole was enlarged conversely, mass-production nature and dependability were able to be raised.
[0037] Finally, it annealed at 300-400 degrees C in hydrogen for 0.1 to 2 hours, and hydrogenation of silicon was completed. Thus, the thin film integrated circuit which has TFT was completed. And it considered as the active matrix liquid crystal display of the MONOSHI rucksack mold which was made to arrange TFT of a large number produced to coincidence in the shape of a matrix, and also formed the circumference circuit on the same substrate.
[0038] [Example 3] The example which produces the thin film integrated circuit which has at least one TFT using the multiple-purpose membrane formation equipment shown in drawing 1 is shown in drawing 3 . First, the multiple-purpose membrane formation equipment used in this example is explained. In this example, 101 was made into the spare room, in order to perform carrying-in taking out of a substrate. moreover -- the processing room which makes 106 the processing room which heats, makes 103 the processing room which forms a silicon nitride film by the plasma-CVD method, uses TEOS as a raw material for 104, and forms the oxidation silicon film by the plasma-CVD method -- carrying out -- 105 -- LPCVD -- it considers as the processing room which forms the amorphous silicon film by law. Moreover, it considered as the processing room which forms the polycrystal silicon film which doped P for 102 with a reduced pressure heat CVD method. Moreover, the gas installation means for introducing the exhaust air means for changing each processing room into a reduced pressure condition and the gas needed further is formed in each processing room.
[0039] A making process is shown below. First, the heat-resistant high crystallization glass plate (a 4 inch angle, a 5 inch angle, or 5x6 inch angle) 201 represented by N0 glass as a substrate is carried in to a spare room 101, and vacuum suction is carried out enough. As for this vacuum suction, it is desirable to carry out until it becomes the almost same pressure as the conveyance room 107 enough carried out in vacuum suction. And a gate valve 110 is opened and the substrate in a spare room 101 is transported to the conveyance room 107 by the robot arm 108. In drawing 1 , the substrate 201 in drawing 3 is shown as 109. In addition, it is called a substrate also including the film currently formed on it below. And the gate valve 112 between the reaction chambers 103 where vacuum suction was similarly mostly carried out to the same pressure is opened, and a substrate is carried in. A gate valve 112 is shut after substrate carrying in, and it sets in this reaction chamber 103, and is a silicon nitride film 200 by the plasma-CVD method The substrate temperature of 350 degrees C, 0.1Torr, and SiH4 NH3 Membranes are formed in a mixed ambient atmosphere. This silicon nitride film is for preventing diffusion of the alkali from a substrate.
[0040] And vacuum suction of the reaction chamber 103 is carried out, and a substrate is transported to the conveyance room 107 where vacuum suction was carried out again by the robot arm 108. And a substrate is conveyed to the reaction chamber 106 where vacuum suction was similarly carried out. In this reaction chamber 106, the oxidation silicon film 203 is formed by the plasma-CVD method which used TEOS as the raw material. Membrane formation conditions are shown below.
TEOS/O2 =10 / 100sccmRF Power Whenever [350 W-set board temperature] 400-degree-C membrane formation pressure 0.25Torr [0041] Moreover, it sets for the above-mentioned reaction and is C two F6. It adds and is SiOFx. The film shown may be formed.
[0042] This oxidation silicon film is formed as a substrate oxide film 203 by 2000-50A in thickness in the field which forms TFT.
[0043] And a substrate is again conveyed in the conveyance room 107, and then a substrate is carried in to a reaction chamber 105. All the things that a conveyance room and each processing room make open and close a gate valve in the case of migration of these substrates after vacuum suction is carried out to the same degree of vacuum (the same reduced pressure condition) are common.
[0044] a reaction chamber 105 -- LPCVD -- 200-2000A of 300-800A of amorphous silicon film 204 is preferably deposited by law. The membrane formation conditions in the LPCVD method are shown below.
Si2H6 100sccmHe Whenever [200sccm stoving temperature] 500 degrees C - 570 degree-C membrane formation pressure 0.3Torr growth rate A part for 50A - 500A/[0045] Here, the polycrystal silicon film with the sufficient property of having the mean particle diameter of 250A - 8000A in a subsequent heat crystallization

process can be obtained by it being important to use the polysilane like a disilane and forming membranes on condition that the above using these.
[0046] Then, in order to take out, the substrate which processing ended is again brought together in a spare room 101, and is taken out to the exterior of equipment.
[0047] This is for carrying out patterning of the amorphous silicon film 204 to the shape of an island, and crystallizing after an appropriate time. This is because it is more efficient to consider as another equipment in order for the time amount which these processes' not being processes under reduced pressure and these processes take to raise the operating ratio of equipment as compared with the time amount which other processes take, since it is extraordinarily long.
[0048] Patterning of the amorphous silicon film 204 performs patterning in the shape of [predetermined] an island using well-known photolithography.
[0049] Heat crystallization is performed by heating from 8 hours at 550 degrees C - 600 degrees C in nitrogen-gas-atmosphere mind for 56 hours. Thus, the crystal of the above big particle size can be obtained by crystallizing at low temperature comparatively.
[0050] Then, in 800 degrees C - 850 degrees C, heat annealing is performed on the highest possible temperature and a concrete target within the limits of the heat-resistant temperature of N0 glass. This process enables it to raise the crystallinity in each crystal grain. Moreover, this process may be performed in an oxidizing atmosphere, for example, dry oxygen, and the thermal oxidation film may be formed in coincidence. When using this thermal oxidation film as gate dielectric film, it is appropriate for that thickness to consider as 500A - 2000A.
[0051] Thus, the substrate which finished crystal growth is again thrown in in equipment from a spare room 101.
[0052] The substrate thrown in from the spare room 101 transports a substrate to a reaction chamber 104 further if needed, by the plasma-CVD method which uses TEOS as a raw material, is shown in drawing 3 (B) and forms the 500-1000A oxidation silicon film 205 preferably 200-1500A in thickness like. Here, TEOS was used as the raw material, and with oxygen, the substrate temperature of 350-600 degrees C, it is 300-450 degrees C preferably, and decomposed and deposited by RF plasma-CVD method. In the pressure ratio of TEOS and oxygen, 0.05 - 0.5torr and RF Power set 1:1-1:3, and a pressure to 100-250W.
[0053] This process may form preferably 350-600 degrees C of substrate temperature as 400-550 degrees C with a reduced pressure CVD method or an ordinary pressure CVD method with ozone gas by using TEOS as a raw material.
[0054] Moreover, it annealed at 400-600 degrees C by the ambient atmosphere of oxygen or ozone after membrane formation for 30 to 60 minutes.
[0055] When membrane formation of the above-mentioned oxidation silicon film 205 performs elevated-temperature annealing after heat crystallization in an oxidizing atmosphere and it uses the thermal oxidation film as gate dielectric film, it cannot be overemphasized that this process becomes unnecessary.
[0056] In this way, as shown in drawing 3 (B), the blocking layer 202 of silicon nitride, the oxidation silicon film 203, the crystalline silicon semi-conductor film 204 by which patterning was carried out to the shape of an island, and the oxidation silicon film 205 can be formed on a glass substrate 201 at a multilayer. If there is not little equipment shown in this drawing 1 , it can make the value of C, N, and O especially in the silicon film three or less [5x1018cm -]. [since each chamber and the conveyance room with a robot arm are divided with the gate valve, respectively an impurity does not mix mutually between each chambers, and]
[0057] When forming the oxidation silicon film 205 used as the above-mentioned gate dielectric film in a reaction chamber 104, it is effective to carry in a substrate to an annealing chamber 106 after the process termination, and to perform RAPITTO thermal annealing by infrared exposure in an N2 O ambient atmosphere. This has effectiveness in decreasing the interface state density of the oxidation silicon film 205 and the silicon field 204 extremely.
[0058] Next, the polycrystal silicon film which doped P used as a gate electrode is formed with the reduced pressure heat CVD on the above-mentioned gate dielectric film at the thickness of 1000A - 4000A.
[0059] Especially the field side to [to the above-mentioned process (i.e., from a substrate)] a silicon semi-conductor layer, gate dielectric film, and a gate electrode is sensitive to interface state density etc., and it is the main parts which determine the property of a device, and without so being exposed to atmospheric air, it is desirable to form membranes continuously and it of it becomes possible by the configuration of this invention.
[0060] From the equipment of this invention, the following processes are taken out outside and performed.
[0061] First, dry etching performs patterning for the polycrystal silicon film which doped P that the gate electrode 217 should be formed. (Drawing 3 (C))

[0062] then, the ion doping method (it is also called the plasma doping method) — every — an impurity (phosphorus) is poured in in self align by using the gate electrode 217 as a mask into the island-like silicon film of TFT. Phosphoretted hydrogen (PH3) was used as doping gas. The dose was set to 1-4x1015cm-2.
[0063] Next, after heating 600 degrees C of substrates in nitrogen-gas-atmosphere mind for 12 hours and activating a dopant, further, in a hydrogen ambient atmosphere, by 400 degrees C, it heat-treats for 1 hour, a hydrogen treating is performed, and the defective level consistency of a semi-conductor layer is decreased.
[0064] then, other equipments — or an interlayer insulation film 210 is again formed in the whole surface using the equipment of drawing 1 . When the equipment of drawing 1 was used, 3000A (0.3 micrometers) formation of the oxidation silicon film was carried out 0.3 micrometers - 1 micrometer in thickness by using TEOS as a raw material here with the plasma-CVD method of this and oxygen, the reduced pressure CVD method with ozone, or the ordinary pressure CVD method, using the reaction chamber 104 of the reactor of drawing 1 again. Substrate temperature was made into 250-450 degrees C, for example, 350 degrees C. After membrane formation, in order to obtain surface surface smoothness, this oxidation silicon film was ground mechanically. This process may perform isotropic dry etching using the reaction chamber prepared in the equipment of drawing 1 . Furthermore, by the spatter, the ITO coat was deposited, patterning of this was carried out, and it considered as the pixel electrode 211. (Drawing 3 (E))
[0065] If it writes and carries out, a thin film integrated circuit can be made to one substrate side of an electro-optic device. Of course, a circumference circuit may be formed on the same substrate at the circuit and coincidence which are shown in this drawing. And the layer insulation object 210 was etched, as shown in drawing F (E), the contact hole was formed in the source/drain of TFT, the wiring 212 and 213 of chromium or titanium nitride was formed, and wiring 213 was connected to the pixel electrode 211. in addition, in this case, it is **** about the source / drain field (island-like silicon) -- it may carry out and a contact hole may be formed. in this case, it is **** about island-like silicon among contact holes -- the area carried out was 30 - 70%. In this case, contact is formed also not only in the top face of the source/drain but in a side face. Hereafter, such contact is called top side contact. In the conventional structure, although even the substrate was etched into the oxidization silicon film of the substrate of parts other than island-like silicon, and a pan by the etching process of a layer insulation object when it was going to form top side contact, a silicon nitride film 200 serves as an etching stopper, and etching stops at this example here.
[0066] In the usual case, although magnitude of a contact hole needed to be made smaller than the source/drain, in top side contact, it can make magnitude of an island smaller than a contact hole conversely, and detailed-ization of an island can do it as a result. Moreover, since the KONTAKU hole was enlarged conversely, mass-production nature and dependability were able to be raised.
[0067] Thus, the thin film integrated circuit which has TFT was completed. And it considered as the active matrix liquid crystal display of the MONOSHI rucksack mold which was made to arrange TFT of a large number produced to coincidence in the shape of a matrix, and also formed the circumference circuit on the same substrate.
[0068] In addition, when a substrate is used as a quartz substrate in the above-mentioned example, the oxidation silicon film of a substrate can be omitted and may also omit the oxidation silicon film of a substrate depending on the case. Moreover, since the thermal resistance of a substrate is high, it is possible to raise the temperature of heat annealing after heat crystallization or the process of thermal oxidation to about 1000 degrees C, and it is possible to obtain the crystalline good silicon film in that case further.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The multiple-purpose substrate processor of an example is shown.
[Drawing 2] The making process of TFT in an example is shown.
[Drawing 3] The making process of TFT in an example is shown.
[Description of Notations]
101-106 .... Processing room
108 ..... Robot arm
109 ..... Substrate
110-115 .... Gate valve
201 ..... Glass substrate
202 ..... Nitriding aluminum film
200 ..... Silicon nitride film
203 ..... Oxidation silicon film
204 ..... Silicon film
205 ..... Oxidation silicon film (gate dielectric film)
206 ..... Gate electrode
209 ..... Anode plate oxide layer
217 ..... Gate electrode
210 ..... Layer insulation object
211 ..... ITO electrode (pixel electrode)
214/215 .... The source / drain electrode

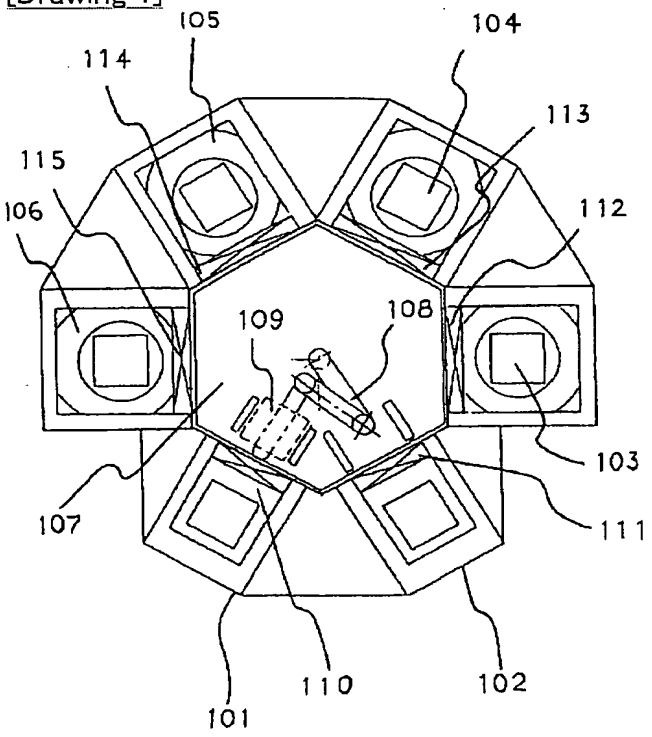
[Translation done.]

* NOTICES *

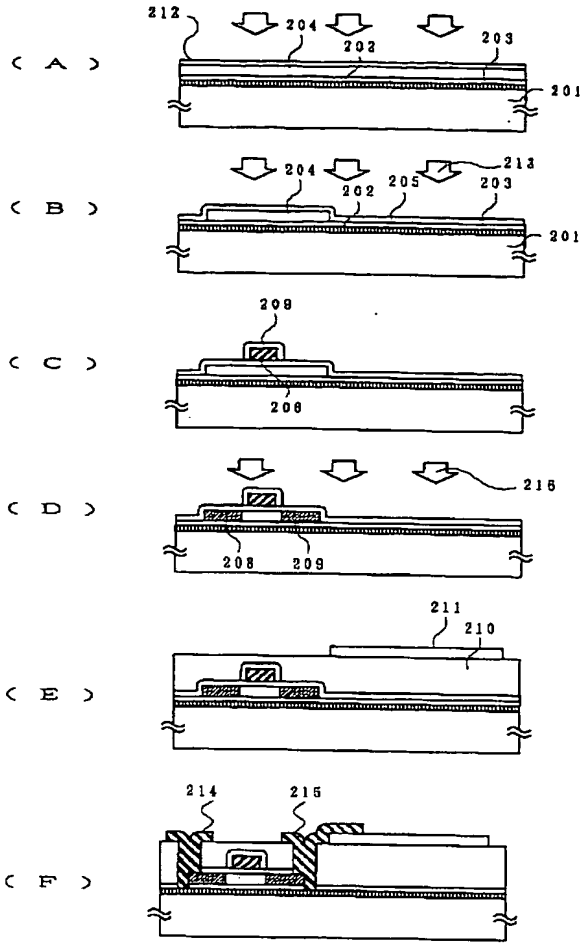
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

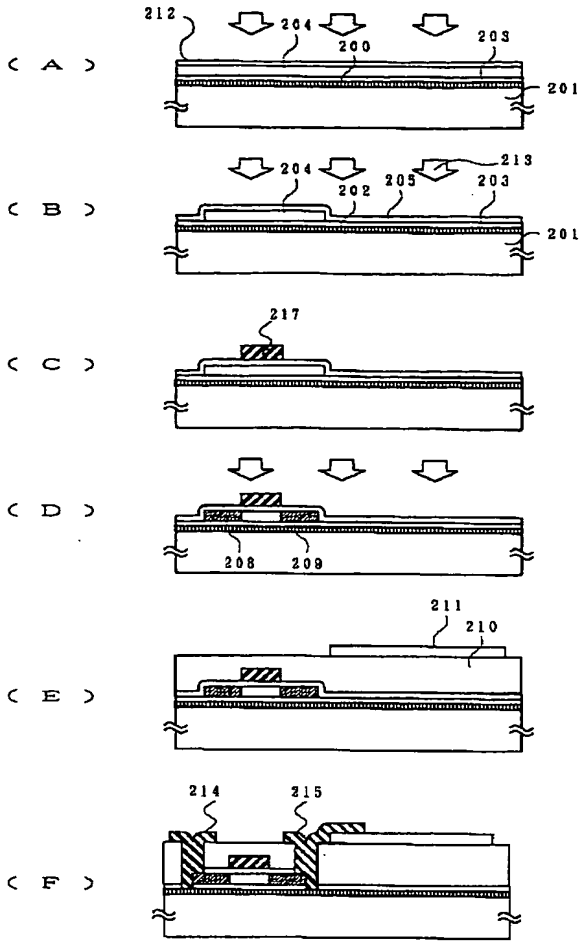
[Drawing 1]



[Drawing 2]


(A)
212
204
202
203
201
(B)
204
213
202
205
203
201
(C)
209
208
(D)
216
208
209
(E)
211
210
(F)
214
215

[Drawing 3]



[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CORRECTION OR AMENDMENT

[Kind of official gazette] Printing of amendment by the convention of 2 of Article 17 of Patent Law
[Section partition] The 2nd partition of the 7th section
[Publication date] October 12, Heisei 13 (2001. 10.12)

[Publication No.] JP,7-183235,A
[Date of Publication] July 21, Heisei 7 (1995. 7.21)
[Annual volume number] Open patent official report 7-1833
[Application number] Japanese Patent Application No. 5-347646
[The 7th edition of International Patent Classification]

H01L 21/205
C23C 16/24
16/40
16/44
16/50
H01L 21/316
21/318

[FI]

H01L 21/205
C23C 16/24
16/40
16/44 E
16/50
H01L 21/316 X
21/318 B

[Procedure revision]
[Filing Date] December 25, Heisei 12 (2000. 12.25)
[Procedure amendment 1]
[Document to be Amended] Specification
[Item(s) to be Amended] Claim
[Method of Amendment] Modification
[Proposed Amendment]
[Claim(s)]
[Claim 1] It is the multi chamber which it has two or more processing rooms equipped with the vacuum pump, and one of said two or more of the processing rooms is the membrane-formation room of the silicon film by the reduced pressure heat CVD, one of said two or more of the processing rooms is the membrane-formation room of the oxidation silicon film by plasma CVD, or a silicon nitride film, and two or more of said processing rooms are connected through the community room equipped with the vacuum pump, and is characterized by for said community room to have the carrier robot of a substrate.
[Claim 2] The multi chamber indicated by claim 1 is a multi chamber characterized by having the optical irradiation chamber, the heat chamber, the sputtering room, or the plasma-etching room.
[Claim 3] It is the multi chamber characterized by said optical exposure being an infrared light exposure or an

excimer laser light exposure in claim 2.
[Claim 4] The approach of the multi chamber characterized by to carry out plasma cleaning at a processing room which is the approach of the multi chamber indicated by any 1 term of claim 1 thru/or claim 3 of operation, and is different from said processing room currently etched [which is etching, and is forming membranes, heating and light-irradiating] while forming membranes, heating and light-irradiating or etching by one of two or more of the processing rooms of said of operation.
[Claim 5] It is the approach of the multi chamber characterized by said plasma cleaning using 3 nitrogen-fluoride (NF3) gas in claim 4 of operation.
[Claim 6] The approach of the multi chamber which is the approach of the multi chamber indicated by any 1 term of claim 1 thru/or claim 3 of operation, and is characterized by conveying the substrate held one of said two or more of the processing rooms in said community room when the indoor pressure in one of said two or more of the processing rooms and the indoor pressure in said community room are the same of operation.
[Claim 7] The approach of the multi chamber which is the approach of the multi chamber indicated by any 1 term of claim 1 thru/or claim 3 of operation, and is characterized by conveying the substrate held at said community room to one of said two or more of the processing rooms when the indoor pressure in one of said two or more of the processing rooms and the indoor pressure in said community room are the same of operation.

[Claim 8] The production approach of the thin film integrated circuit characterized by performing the process which forms the amorphous silicon film with the reduced pressure heat CVD, the process which forms gate dielectric film by plasma CVD, the process which forms an interlayer insulation film, the process which crystalizes said amorphous silicon film, and the process which carries out an optical exposure at said gate dielectric film in the multi chamber which has two or more processing rooms.
[Claim 9] Have two or more processing rooms equipped with the vacuum pump, and said two or more processing rooms are connected through the community room equipped with the vacuum pump. Said community room is the production approach of the thin film integrated circuit using the multi chamber which has the carrier robot of a substrate. The production approach of the thin film integrated circuit characterized by crystallizing said amorphous silicon film after forming the amorphous silicon film with the reduced pressure heat CVD in said multi chamber, forming gate dielectric film by plasma CVD on said amorphous silicon film and carrying out an optical exposure at said gate dielectric film.
[Claim 10] It is the production approach of the thin film integrated circuit characterized by the optical exposure after said gate-dielectric-film formation being an infrared light exposure in claim 8 or claim 9.
[Claim 11] The production approach of the thin film integrated circuit characterized by performing said infrared light exposure in a dinitrogen oxide (N2O) gas ambient atmosphere in claim 10.
[Claim 12] The production approach of the thin film integrated circuit characterized by crystallizing said amorphous silicon film by excimer laser light exposure in claim 8 or claim 9.
[Procedure amendment 2]
[Document to be Amended] Specification
[Item(s) to be Amended] 0005
[Method of Amendment] Modification
[Proposed Amendment]
[0005]
[Means for Solving the Problem] In order to produce the semiconductor device which has the barrier layer which consists of polycrystal silicon with a sufficient property, the multiple-purpose substrate processor of this invention Have the processing room in which two or more reduced pressure is possible, and said two or more processing rooms are connected through the community room which can be decompressed. It has a means for conveying a substrate between each processing room in said community room. Membrane formation of the silicon film by the reduced pressure heat CVD is possible for at least one of said two or more processing rooms, and membrane formation of the oxidation silicon film by plasma CVD or a silicon nitride film is possible for at least one of said two or more processing rooms, Or have the processing room in which two or more reduced pressure is possible, and said two or more processing rooms are connected through the community room which can be decompressed. It has a means for conveying a substrate between each processing room in said community room. Membrane formation of the silicon film by the reduced pressure heat CVD is possible for at least one of said two or more processing rooms, and membrane formation of the oxidation silicon film by plasma CVD is possible for at least one of said two or more processing rooms. At least one of said two or more

processing rooms is characterized [the / biggest] by membrane formation of the silicon nitride film by plasma CVD being possible.
[Procedure amendment 3]
[Document to be Amended] Specification
[Item(s) to be Amended] 0009
[Method of Amendment] Modification
[Proposed Amendment]
[0009] The concrete example of this invention is shown in drawing 1. The equipment shown in drawing 1 can be used for multiple purposes, and can be combined by the number which needs the processing room which performs membrane formation to need and annealing treatment. As a substrate processed with the equipment shown in drawing 1, a glass substrate, a silicon substrate, other insulating substrates, and a semi-conductor substrate can be used. That is, if it is the substrate which has an insulating front face, it can use. For example, if it is electro-optic devices, such as a liquid crystal display of a active-matrix mold, and image sensors, it is common to use a cheap glass substrate.
[Procedure amendment 4]
[Document to be Amended] Specification
[Item(s) to be Amended] 0056
[Method of Amendment] Modification
[Proposed Amendment]
[0056] In this way, as shown in drawing 3 (B), the blocking layer 202 of silicon nitride, the oxidation silicon film 203, the crystalline silicon semi-conductor film 204 by which patterning was carried out to the shape of an island, and the oxidation silicon film 205 can be formed on a glass substrate 201 at a multilayer. Since each chamber and the conveyance room with a robot arm are divided with the gate valve, respectively, an impurity cannot mix mutually between each chambers and the equipment shown in this drawing 1 can make the value of C, N, and O especially in the silicon film at least below 5x10^(18) cm^ (-3).
[Procedure amendment 1]
[Document to be Amended] Specification
[Item(s) to be Amended] 0056
[Method of Amendment] Modification
[Proposed Amendment]
[0056] In this way, as shown in drawing 3 (B), the blocking layer 202 of silicon nitride, the oxidation silicon film 203, the crystalline silicon semi-conductor film 204 by which patterning was carried out to the shape of an island, and the oxidation silicon film 205 can be formed on a glass substrate 201 at a multilayer. Since each chamber and the conveyance room with a robot arm are divided with the gate valve, respectively, an impurity cannot mix mutually between each chambers and the equipment shown in this drawing 1 can make the value of C, N, and O especially in the silicon film three or less [at least 5x1018cm -].

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12) 公開特許公報（Ａ）　(11)特許出願公開番号

特開平7－183235

(43)公開日　平成７年(1995)７月21日

(51)Int.Cl.[6]		識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０１Ｌ	21/205				
Ｃ２３Ｃ	16/24				
	16/40				
	16/44		E		
	16/50				

審査請求　未請求　請求項の数６　ＦＤ　（全 11 頁）　最終頁に続く

(21)出願番号　特願平5－347646

(22)出願日　平成５年(1993)12月24日

(71)出願人　000153878
株式会社半導体エネルギー研究所
神奈川県厚木市長谷398番地

(72)発明者　大谷　久
神奈川県厚木市長谷398番地　株式会社半導体エネルギー研究所内

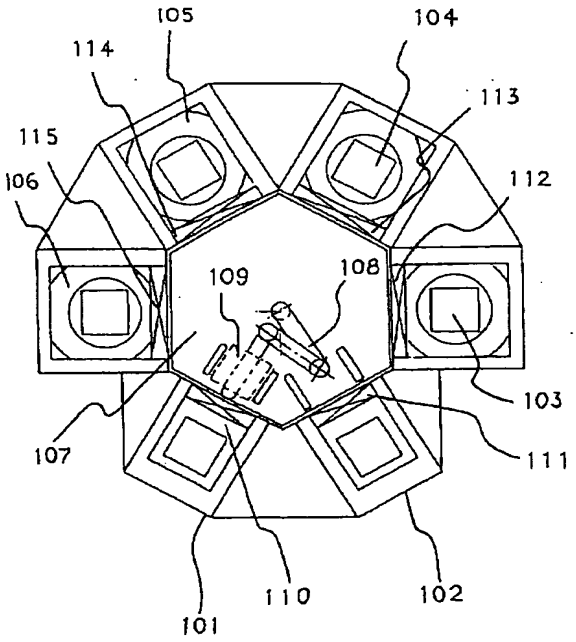
(72)発明者　島田　浩行
神奈川県厚木市長谷398番地　株式会社半導体エネルギー研究所内

(72)発明者　坂間　光範
神奈川県厚木市長谷398番地　株式会社半導体エネルギー研究所内

最終頁に続く

(54)【発明の名称】　多目的基板処理装置およびその動作方法および薄膜集積回路の作製方法

(57)【要約】
【目的】　基板上に薄膜を形成したり、形成した薄膜に対してアニールを行ったりする各種処理を機密性を保ったままで連続的に行う。
【構成】　基板を搬送するためのロボットアーム１０８を備えた搬送室１０７と、該搬送室を介して連結された複数の処理室（チャンバー）１０３～１０６を備え、搬送室を介して基板１０９を各処理室に搬入搬出することで、必要とする処理を機密性を保持した状態で連続して行う。そして処理室の少なくとも一つが減圧熱ＣＶＤ法による珪素膜の作製機能を有し、他の処理室の少なくとも一つがプラズマＣＶＤ法による酸化珪素膜あるいは窒化珪素膜の作製機能を有することを特徴とする。



1

【特許請求の範囲】
【請求項１】複数の減圧可能な処理室を有し、
前記複数の処理室は減圧可能な共通室を介して連結されており、
前記共通室には各処理室間において基板を搬送するための手段を有し、
前記複数の処理室の内の少なくとも一つは減圧熱ＣＶＤによる珪素膜の成膜が可能であり、
前記複数の処理室の内の少なくとも一つはプラズマＣＶＤによる酸化珪素膜あるいは窒化珪素膜の成膜が可能であることを特徴とする多目的基板処理装置。
【請求項２】複数の減圧可能な処理室を有し、
前記複数の処理室は減圧可能な共通室を介して連結されており、
前記共通室には各処理室間において基板を搬送するための手段を有し、
前記複数の処理室の内の少なくとも一つは減圧熱ＣＶＤによる珪素膜の成膜が可能であり前記複数の処理室の内の少なくとも一つはプラズマＣＶＤによる酸化珪素膜の成膜が可能であり、
前記複数の処理室の内の少なくとも一つはプラズマＣＶＤによる窒化珪素膜の成膜が可能であることを特徴とする多目的基板処理装置。
【請求項３】複数の減圧可能な処理室を有し、
前記複数の処理室は減圧可能は共通室を介して連結されており、
前記共通室には各処理室間において基板を搬送するための手段を有した多目的基板処理装置の動作方法であって、
同一圧力に保持された状態において、いずれか一つの処理室に保持された基板を共通室に移送すること、
あるいは共通室に保持された基板をいずれか一つの処理室に移送すること、
及び前記処理室の内の少なくとも一つにおいて減圧熱ＣＶＤにより珪素膜の成膜を行なうこと、
及び前記処理室の内の少なくとも一つにおいてプラズマＣＶＤにより酸化珪素膜あるいは窒化珪素膜の成膜を行なうこと、
を特徴とする多目的基板処理装置の動作方法。
【請求項４】複数の減圧可能な処理室を有し、
前記複数の処理室は減圧可能は共通室を介して連結されており、
前記共通室には各処理室間において基板を搬送するための手段を有した多目的基板処理装置の動作方法であって、
同一圧力に保持された状態において、いずれか一つの処理室に保持された基板を共通室に移送すること、
あるいは共通室に保持された基板をいずれか一つの処理室に移送すること、
及び前記処理室の内の少なくとも一つにおいて減圧熱ＣＶＤにより珪素膜の成膜を行なうこと、
及び前記処理室の内の少なくとも一つにおいてプラズマＣＶＤにより酸化珪素膜の成膜を行なうこと、
及び前記処理室の内の少なくとも一つにおいてプラズマＣＶＤにより窒化珪素膜の成膜を行なうこと、
を特徴とする多目的基板処理装置の動作方法。
【請求項５】珪素半導体層を含めた多層成膜をする工程と、
ゲイト絶縁膜を形成する工程と、
層間絶縁膜を形成する工程と、
を複数の反応容器を有する多目的基板処理装置を用いて処理し、
前記工程の内珪素半導体層は減圧熱ＣＶＤにより作製され、
前記工程の内ゲイト絶縁膜層はプラズマＣＶＤにより作製された、ことを特徴とする薄膜集積回路の作製方法。
【請求項６】複数の減圧可能な処理室を有し、
前記複数の処理室は減圧可能な共通室を介して連結されており、
前記共通室には各処理室間において基板を搬送するための手段を有した多目的基板処理装置を用いた薄膜集積回路の作製方法であって、
窒化珪素膜をプラズマＣＶＤで第１の処理室で形成する工程と、
酸化珪素膜をプラズマＣＶＤで第２の処理室で形成する工程と、
珪素膜を減圧熱ＣＶＤ法で第３の処理室で形成する工程と、
酸化形成膜を第４の処理室で形成する工程と、
を有する薄膜集積回路の作製方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は基板上あるいは基板表面に多結晶珪素からなる半導体装置を形成する装置に関する。特に外気に曝することなく連続して行なわれる必要のあるプロセスを行なうことのできる装置に関する。また薄膜集積回路の作製に利用することのできる多目的基板処理装置に関する。
【０００２】
【従来の技術】半導体基板やガラス基板を用いた集積回路が知られている。前者としてはＩＣやＬＳＩが知られており、後者としてはアクティブマトリックス型の液晶表示装置が知られている。このような集積回路を形成するには、各種プロセスを連続して行なう必要がある。例えば絶縁ゲイト型電界効果半導体装置を形成する場合であれば、チャネルが形成される半導体領域とそれに接して設けられるゲイト絶縁膜とを外部に取り出すことなく連続して形成することが望まれる。また各種プロセスを効率良く連続して行なうことが工業上必要である。
【０００３】これらの製造には、一つの装置内で成膜工

2

程を連続して行なうことが望ましいが、従来の製造装置は非晶質珪素を用いた半導体装置を目的とした製造装置、あるいは単結晶珪素を用いた半導体装置を目的とした製造装置しか存在せず、多結晶珪素を用いた半導体装置に適した装置及びそれを用いた製造方法は確立されていなかった。

【０００４】

【発明が解決しようとする課題】本発明は、多結晶珪素を用いた半導体装置の作製に必要とされる各種プロセスを一つの装置で連続して処理することのできる多目的に利用できる基板処理装置を提供することを目的とする。特に多結晶珪素を用いた半導体を特性良く作製するために、ポリシランを用いた減圧熱ＣＶＤによる珪素膜の形成手段を有すること及び、その上下の両方あるいはそのどちらかに接して設ける必要がある絶縁膜をプラズマＣＶＤによって形成することが可能であることが前記基板処理装置においては必須の構成である。

【０００５】

【課題を加熱するための手段】多結晶珪素からなる活性層を有する半導体装置を特性良く作製するために、本発明の多目的基板処理装置は、複数の減圧可能な処理室を有し、前記複数の処理室は減圧可能な共通室を介して連結されており、前記共通室には各処理室間において基板を搬送するための手段を有し、前記複数の処理室の内の少なくとも一つは減圧熱ＣＶＤによる珪素膜の成膜が可能であり前記複数の処理室の内の少なくとも一つはプラズマＣＶＤによる酸化珪素膜あるいは窒化珪素膜の成膜が可能であること、あるいは、複数の減圧可能な処理室を有し、前記複数の処理室は減圧可能な共通室を介して連結されており、前記共通室には各処理室間において基板を搬送するための手段を有し、前記複数の処理室の内の少なくとも一つは減圧熱ＣＶＤによる珪素膜の成膜が可能であり前記複数の処理室の内の少なくとも一つはプラズマＣＶＤによる酸化珪素膜の成膜が可能であり、前記複数の処理室の内の少なくとも一つはプラズマＣＶＤによる窒化珪素膜の成膜が可能であることをその最も大きな特徴とする。

【０００６】また多結晶珪素からなる活性層を有する半導体装置を特性良く作製するために、本発明の多目的基板処理装置の動作方法は、同一圧力に保持された状態において、いずれか一つの処理室に保持された基板を共通室に移送すること、あるいは共通室に保持された基板をいずれか一つの処理室に移送すること、及び前記処理室の内の少なくとも一つにおいて減圧熱ＣＶＤにより珪素膜の成膜を行なうこと、及び前記処理室の内の少なくとも一つにおいてプラズマＣＶＤにより酸化珪素膜の成膜あるいは窒化珪素膜の成膜を行なうことあるいは、同一圧力に保持された状態において、いずれか一つの処理室に保持された基板を共通室に移送すること、あるいは共通室に保持された基板をいずれか一つの処理室に移送すること、及び前記処理室の内の少なくとも一つにおいて減圧熱ＣＶＤにより珪素膜の成膜を行なうこと、及び前記処理室の内の少なくとも一つにおいてプラズマＣＶＤにより酸化珪素膜の成膜を行なうこと及び前記処理室の内の少なくとも一つにおいてプラズマＣＶＤにより窒化珪素膜の成膜を行なうことを特にその特徴とする。

【０００７】上述の様な構成をとる必要性について簡単に述べると、従来は非晶質珪素を用いた半導体装置の製造プロセスが専ら多結晶珪素を用いた半導体装置の製造に用いられてきた。その際に、珪素膜の成膜に用いられているのはグロー放電を用いたプラズマＣＶＤであり、その様にして作製された珪素膜は多量の水素を含んでおり、結晶化させる際の水素の放出等に伴って膜の状態が大きく変化してしまい、折角多数の処理室を持った連続成膜の様な構成をとっても十分な特性を有する多結晶珪素からなる半導体装置を得ることは困難であることが実験の結果判明した。この問題点を解決するためにはＬＰＣＶＤを用い、原料ガスとしてジシランの如きポリシランを用いることが有効であることがわかった。

【０００８】しかしながら、既存の製造装置及び製造プロセスにおいては、ＬＰＣＶＤを用いた場合であっても、大気中に一度暴露してしまうため、特性の良い界面を形成できず、やはり十分な特性を有する多結晶珪素からなる半導体装置を得ることは困難であった。そこで、最も重要なきれいな界面の接合を実現するためには、ＬＰＣＶＤによる珪素膜の成膜と、その上下の両方あるいはその一方に接して設ける必要がある絶縁膜を、連続的に大気に開放することなく成膜することで、特性の飛躍的な向上が可能であることが発明者らの実験により判明した。この絶縁膜の成膜方法としては、発明者らの実験結果から、特性及びスループット等を考慮してプラズマＣＶＤによる方法がベストであるとの結論に達した。

【０００９】本発明の具体的な例を図１に示す。図１に示す装置は多目的に利用できるものであって、必要とする成膜やアニール処理を施す処理室を必要とする数で組み合わせることができる。図１に示す装置で処理される基板はとしてが、ガラス基板、シリコン基板、その他絶縁基板や半導体基板を用いることができる。即ち、絶縁表面を有する基板であれば用いることができる。例えば、アクティブマトリクス型の液晶表示装置やイメージセンサー等の電気光学装置であれば安価なガラス基板を用いるのが一般的である。

【００１０】例えば１０７を共通室である基板の搬送室とし、基板の各種処理を行なう処理室の内、１０１と１０２とを予備室とし、一方を基板の搬入用に用い、他の一方を基板の搬出用に用いる。また、１０３は絶縁膜を形成するためのプラズマＣＶＤ装置とし、１０４を非晶質珪素を成膜するための減圧熱ＣＶＤ装置とし、１０５を熱酸化膜を形成するための加熱炉とし、１０６を光照射によるアニールを行なうためのアニール炉とする、と

5　　6

いった構成を採ることができる。なお、予備室も基板の搬入や搬出を行なう機能を有するという意味で処理室ということができる。

【００１１】このような組み合わせは任意に行なえるものである。これら組み合わせのできる要素としては、プラズマＣＶＤ、減圧熱ＣＶＤ（以下本明細書においてはＬＰＣＶＤと省略する）、光ＣＶＤ、マイクロ波ＣＶＤ、加熱炉、光照射によるアニール炉、スパッタリング、プラズマアニール、プラズマエッチングを挙げることができる。

【００１２】

【実施例】

〔実施例１〕本実施例の構成を図１に示す。本実施例に＊おいては、１０１と１０２が予備室であり、基板の出し入れを行なう機能を有する。これらのチャンバーは、複数の基板が収められたカセットを保持する機能を有する。また当然不活性ガスの導入手段やクリーニングガスの導入手段、さらにはガス排気手段を有している。

【００１３】１０３～１０６は処理室であり、１０３と１０６とがプラズマＣＶＤ装置であり、１０４が温度調節チャンバーである。温度調節チャンバーとは、基板を所定の温度に加熱する機能を有するものであり、他のチャンバーでの成膜に先立ち、予め基板を加熱しておくために使用される。各処理室の仕様を下記表１に示す。

【００１４】

【表１】

	１０６	１０５	１０４	１０３
処理内容	ＰＣＶＤ	予備加熱 ＲＴＰ	ＰＣＶＤ ＬＰＣＶＤ	ＰＣＶＤ
ＲＦ電源	13.56MHz 500 W	――――	13.56MHz 500 W	13.56MHz 500 W
電　極	平行平板	平行平板	平行平板	平行平板
プロセスガス	N_2. SiH_4. NH_3 $Al(CH_3)_3$	N_2O. N_2. NH_3. O_2	N_2. SiH_4. H_2 Si_2H_6. Si_3H_8	N_2. TEOS. O_2 C_2F_6
クリーニングガス	NF_3 ＋N_2	――――	NF_3 ＋N_2	NF_3 ＋N_2
基板加熱温度	４５０℃	４５０℃	５５０℃	６００℃
膜	Si_2H_4 ＡｌＮ	――――	Ｓｉ	SiO_2 SiF_x
排気設備	到達圧力 5×10^{-7}Torr	到達圧力 5×10^{-8}Torr	到達圧力 5×10^{-5}Torr	到達圧力 5×10^{-8}Torr

尚、基板サイズとしては、４インチ角、５インチ角、５×６インチ角を利用することができる。

【００１５】１０７は基板の搬送室であり、ロボットアーム１０８によって基板が各チャンバー間を搬送される。ロボットアーム１０８は基板（１０９で示される）を１枚づつ予備室１０１あるいは１０２から取り出し、必要とする反応室に移動させる機能を有する。当然各処理室間においても基板を移動させることができる。また、この搬送室にも排気手段が設けられており、必要とする真空度にすることができる。

【００１６】各チャンバー間の基板の移動は以下のようにして行なわれる。例えば、予備室１０１に保持される基板を処理室１０３と１０４とで処理し、予備室１０２に搬入する場合を考える。この場合まず、

（１）予備室１０１と搬送室１０７とを同一減圧状態（高真空状態が望ましい）とし、その状態においてゲイトバルブ１１０を開け、ロボットアーム１０８によって基板１０９を搬送室に取り出す。その後ゲイトバルブ１１０は閉める。

（２）搬送室１０７と処理室１０３とを同一減圧状態とし、その状態においてゲイトバルブ１１２を開け、ロボットアーム１０８に保持された基板１０９をプロセス室に搬入する。その後ゲイトバルブ１１２は閉める。

（３）処理室１０３において所定のプロセスが行なわれる。

（４）処理室１０３でのプロセス終了後、処理室１０３の真空度を搬送室１０７と同一減圧状態とし、その後ゲイトバルブ１１２を開け、ロボットアーム１０８によって基板を搬送室１０７に搬出する。そしてゲイトバルブ１１２は閉める。

（５）搬送室１０７と処理室１０４とを同一減圧状態とし、その状態においてゲイトバルブ１１３を開け、ロボットアーム１０８に保持された基板を処理室１０４に搬入する。その後ゲイトバルブは閉める。

（６）処理室１０４において所定のプロセスが行なわれる。

（７）処理室１０４でのプロセス終了後、処理室１０４の真空度を搬送室１０７と同一減圧状態とし、その後ゲ

イトバルブ１１３を開け、ロボットアーム１０８によって基板を搬送室１０７に搬出する。そしてゲイトバルブ１１３は閉める。

（８）搬送室１０７と予備室１０２とを同一減圧状態とし、その状態においてゲイトバルブ１１１を開け、ロボットアーム１０８によって基板を予備室１０２に搬入し、その後ゲイトバルブ１１１を閉める。

【００１７】以上のようにして、一枚の基板を外気に曝すことなく、２回またはそれ以上の処理を連続的に行なうことができる。これらの処理としては成膜だけでなく、アニール等も行なえることは有用である。

【００１８】上記（１）～（８）の工程を繰り返すことにより、予備室１０１に搬入されているカートリッジに保持された複数の基板を次から次へと連続的に処理することができる。そして、処理の終了した基板は、予備室１０２のカートリッジに自動的に保持されることになる。また上記の成膜工程において、処理室１０３が稼働中において処理室１０４をクリーニングし、逆に処理室１０４が稼働中に処理室１０３をクリーニングすることによって、全体の動作を止めることなく、クリーニングを行いながら連続した処理工程を行うことができる。このようなクリーニングとしては、NF_3によるチャンバー内のプラズマクリーニングを挙げることができる。

【００１９】〔実施例２〕図１に示す多目的成膜装置を用いて多結晶珪素を活性層とするＴＦＴを少なくとも一つ有する薄膜集積回路を作製する例を図２に示す。まず、本実施例において用いる多目的成膜装置について説明する。本実施例においては、１０１、１０６を基板の搬入搬出を行なうために予備室とした。特にここでは１０１を基板搬入用に、１０６を基板搬出用とした。また１０４を赤外光の短時間照射によるラピットサーマルアニールプロセス（ＲＴＡまたはＲＴＰという）、または予備加熱を行なう処理室とし、１０３をプラズマＣＶＤ法によって窒化アルミニウムを主成分とする膜（窒化アルミオキサイドを以下窒化アルミニウムという）または窒化珪素膜を成膜する処理室とし、１０４をＴＥＯＳを原料としてプラズマＣＶＤ法により酸化珪素膜を成膜する処理室とし、１０５をＬＰＣＶＤ法により非晶質珪素膜を成膜する処理室とする。また各処理室には、各処理室を減圧状態にするための排気手段、さらには必要とされるガスを導入するためのガス導入手段が設けられている。

【００２０】以下に作製工程を示す。まず、基板としてコーニング７０５９等のガラス基板（４インチ角、５インチ角または５×６インチ角）２０１を予備室１０１に搬入し、十分真空引きをする。この真空引きは、十分真空引きをされた搬送室１０７とほぼ同一の圧力になるまで行なうのが好ましい。そしてゲイトバルブ１１０を開け、ロボットアーム１０８によって、予備室１０１内の基板を搬送室１０７に移送する。図１においては、図２における基板２０１は１０９として示されている。なお、以下においてはその上に成膜されている膜も含めて基板という。そして、同じくほぼ同一圧力に真空引きがされた反応室１０３との間のゲイトバルブ１１２を開け、基板を搬入する。基板搬入後にゲイトバルブ１１２を閉め、この反応室１０３内において、厚さ２０００～５０００Åの窒化アルミニウム膜２０２をプラズマＣＶＤ法で形成する。成膜は、$Al(C_4H_9)$、または$Al(CH_3)$とN_2とを用いて行なう。また、N_2Oを微量添加して熱膨張歪を緩和させてもよい。

【００２１】窒化アルミニウム膜２０２の成膜後は、反応室１０３を搬送室１０７と同じ真空度まで真空引きする。そして、ゲイトバルブ１１２を開き、ロボットアーム１０８によって基板を搬送室に基板を移送する。次に同じく真空引きのされたアニール室１０４に基板を搬入する。このアニール室１０４では、赤外線の照射によるラピットサーマルアニール（ＲＴＡ）が行なわれる。このアニールは、窒素、アンモニア（NH_3）、もしくは亜酸化窒素（N_2O）の雰囲気中で行なわれ、短時間に窒化アルミニウム膜を急速に加熱するものである。このアニールによって、窒化アルミニウム膜は透明となり、またその絶縁性や熱伝導性が向上する。また、ガラス基板からのナトリューム等の不純物の半導体への進入を防ぐには、窒化珪素膜を形成してもよい。この場合、窒化珪素膜をプラズマＣＶＤ法により、基板温度３５０℃、０．１Ｔｏｒｒ、SiH_4とNH_3との混合雰囲気で成膜する。

【００２２】そして、反応室１０４を真空引きし、ロボットアーム１０８によって、基板を再び真空引きがされた搬送室１０７に移送する。そして同じく真空引きがされた反応室１０６に基板を搬送する。この反応室１０６ではＴＥＯＳを原料としたプラズマＣＶＤ法で酸化珪素膜２０３が成膜される。成膜条件を以下に示す。

ＴＥＯＳ／O_2	＝１０／１００ｓｃｃｍ
ＲＦパワー	３５０Ｗ
基板温度	４００℃
成膜圧力	０．２５Ｔｏｒｒ

また、上記反応において、C_2F_6を添加して、SiO_xF_yで示される膜を形成してもよい。

【００２３】この酸化珪素膜はＴＦＴを形成する面に下地酸化膜２０３として厚さ２０００～５０Åに成膜される。この反応室１０６で成膜された酸化珪素膜２０３をアニール室１０４に搬送し、ラピットサーマルアニールを行なってもよい。

【００２４】そして、再び基板を搬送室１０７に搬送し、次に反応室１０５に基板を搬入する。これら基板の移送の際において、搬送室とそれぞれの処理室とは同一真空度（同一減圧状態）に真空引きがされた上でゲイトバルブを開閉させることは全て共通である。

【００２５】反応室１０５では、ＬＰＣＶＤ法によって

非晶質珪素膜２０４を１００～１５００Å、好ましくは３００～８００Å堆積する。ＬＰＣＶＤ法での成膜条件を以下に示すが、ここで重要なのはジシランの如きポリシランを用いてＬＰＣＶＤで成膜することであり、従来の非晶質珪素を用いた半導体装置の製造に用いられていたグロー放電によるプラズマＣＶＤ法と比較して、結晶化後の多結晶珪素膜の特性を飛躍的に向上させることが可能である。その際の成膜条件は、代表的には

Si_2H_6	１００～５００ｓｃｃｍ
Ｈｅ	５００ｓｃｃｍ
成膜温度	４３０℃～５００℃
成膜圧力	０．１～１Ｔｏｒｒ

【００２６】さらに反応室１０６に基板を移送し、ＴＥＯＳを原料とするプラズマＣＶＤ法によって、酸化珪素膜２１２を５００～１５００Å程度堆積する。この膜は珪素膜の保護膜として機能する。成膜条件を以下に示す。

ＴＥＯＳ／O_2	＝１０／１００ｓｃｃｍ
ＲＦパワー	３００Ｗ
基板温度	３５０℃
成膜圧力	０．２５Ｔｏｒｒ

かくして、図２（Ａ）に示す如くガラス基板２０１上に窒化アルミニューム、または窒化珪素のブロッキング層２０２、酸化珪素膜２０３、非晶質珪素半導体膜２０４、保護膜２１２を連続して多層に形成することができる。この図１に示す装置は、各チャンバーとロボットアームのある搬送室とはそれぞれゲイトバルブで仕切られているので、個々のチャンバー間において不純物が相互に混入することがなく、特に珪素膜中におけるＣ、Ｎ、Ｏの値を少なくなくと$5\times10^{18}cm^{-3}$以下とすることができる。

【００２７】次に基板を予備室１０１から外部に出し、アイランド状珪素領域２０４を形成するためのパターニングを行なう。そして、図２（Ｂ）に示しように厚さ２００～１５００Å、好ましくは５００～１０００Åの酸化珪素膜２０５を形成する。この酸化珪素膜はゲイト絶縁膜としても機能する。そのためその作製には十分な注意が必要である。ここでは、ＴＥＯＳを原料とし、酸素とともに基板温度３５０～６００℃、好ましくは３００～４５０℃で、ＲＦプラズマＣＶＤ法で分解・堆積した。ＴＥＯＳと酸素の圧力比は１：１～１：３、また、圧力は０．０５～０．５ｔｏｒｒ、ＲＦパワーは１００～２５０Ｗとした。この工程は、搬入室１０１より、基板を搬入し、前記したとは別の操作をして反応室１０６で行なってもよい。あるいはＴＥＯＳを原料としてオゾンガスとともに減圧ＣＶＤ法もしくは常圧ＣＶＤ法によって、基板温度を３５０～６００℃、好ましくは４００～５５０℃として形成してもよい。成膜後、酸素もしくはオゾンの雰囲気で４００～６００℃で３０～６０分アニールした。

【００２８】上記ゲイト絶縁膜となる酸化珪素膜２０５を反応室１０６で成膜する場合は、その工程終了後、基板をアニール室１０４に搬入し、赤外線の照射によるラピットサーマルアニールをN_2、Ｏ雰囲気で行なうことは有効である。これは、酸化珪素膜２０５と珪素領域２０４との界面準位を減少させることに極めて効果がある。

【００２９】そして、図２（Ｂ）に示すようにＫｒＦエキシマーレーザー２１３（波長２４８ｎｍまたは３０８ｎｍ、パルス幅２０ｎｓｅｃ）を照射して、珪素領域２０４を結晶化させた。レーザーのエネルギー密度は２００～４００ｍＪ／cm^2、好ましくは２５０～３００ｍＪ／cm^2とし、また、レーザー照射の際には基板を３００～５００℃に加熱した。このようにして形成された珪素膜２０４の結晶性をラマン散乱分光法によって調べたところ、単結晶珪素のピーク（５２１cm^{-1}）とは異なって、５１５cm^{-1}付近に比較的ブロードなピークが観測され、結晶性半導体例えば多結晶半導体となっていることが判明した。その後、水素中で３５０℃で２時間アニールした。この結晶化の工程は、加熱によることで行なってもよい。

【００３０】その後、厚さ２０００Å～１μｍのアルミニウム膜を電子ビーム蒸着法によって形成して、これをパターニングし、ゲイト電極２０６を形成した。アルミニウムにはスカンジウム（Ｓｃ）を０．１５～０．２重量％ドーピングしておいてもよい。次に基板をｐＨ≒７、１～３％の酒石酸のエチレングリコール溶液に浸し、白金を陰極、このアルミニウムのゲイト電極を陽極として、陽極酸化をおこなった。陽極酸化は、最初一定電流で２２０Ｖまで電圧を上げ、その状態で１時間保持して終了した。本実施例では定電流状態では、電圧の上昇速度は２～５Ｖ／分が適当であった。このようにして、厚さ１５００～３５００Å、例えば、２０００Åの陽極酸化物２０９を形成した。（図２（Ｃ））

【００３１】また高温での熱処理を行なう場合には、アルミニウムの代わりにタンタルを用いればよい。

【００３２】その後、イオンドーピング法（プラズマドーピング法ともいう）によって、各ＴＦＴのアイランド状珪素膜中に、ゲイト電極部をマスクとして自己整合的に不純物（燐）を注入した。ドーピングガスとしてはフォスフィン（PH_3）を用いた。ドーズ量は、１～４×$10^{15}cm^{-2}$とした。

【００３３】さらに、図２（Ｄ）に示すようにＫｒＦエキシマーレーザー（波長２４８ｎｍまたは３０８ｎｍ、パルス幅２０ｎｓｅｃ）２１６を照射して、上記不純物領域の導入によって結晶性の劣化した部分の結晶性を改善させた。レーザーのエネルギー密度は１５０～４００ｍＪ／cm^2、好ましくは２００～２５０ｍＪ／cm^2であった。こうして、Ｎ型不純物（燐）領域２０８、２０９を形成した。これらの領域のシート抵抗は２００～８００Ω／□であった。本工程において、レーザーを用

いるかわりに、フラッシュランプを使用して短時間に１０００～１２００℃（珪素モニターの温度）まで上昇させ、試料を加熱する、いわゆるＲＴＰ（ラピッド・サーマル・プロセス）を用いてもよい。

【００３４】その後、再び図１の装置を用い、全面に層間絶縁物２１０として、図１の反応装置の反応室１０４を再び用い、ＴＥＯＳを原料として、これと酸素とのプラズマＣＶＤ法、もしくはオゾンとの減圧ＣＶＤ法あるいは常圧ＣＶＤ法によって酸化珪素膜を厚さ０．３μｍ～１μｍここでは３０００Å（０．３μｍ）形成した。基板温度は２５０～４５０℃、例えば、３５０℃とした。成膜後、表面の平坦性を得るため、この酸化珪素膜を機械的に研磨した。この工程は、図１の装置内に設けられた反応室を用いて等方性ドライエッチングを行なってもよい。さらに、スパッタ法によってＩＴＯ被膜を堆積し、これをパターニングして画素電極２１１とした。（図２（Ｅ））

【００３５】かくすると、図２の電気光学装置の一方の基板側に薄膜集積回路を作ることができる。勿論、この図面に示す回路と同時に周辺回路を同一基板上に形成してもよい。そして、層間絶縁物２１０をエッチングして、図２（Ｅ）に示すようにＴＦＴのソース／ドレインにコンタクトホールを形成し、クロムもしくは窒化チタンの配線２１２、２１３を形成し、配線２１３は画素電極２１１に接続させた。なお、この際には、ソース／ドレイン領域（アイランド状珪素）をはみだしてコンタクトホールを形成してもよい。この場合にはコンタクトホールのうち、アイランド状珪素をはみだした面積は３０～７０％であった。この場合には、ソース／ドレインの上面のみならず、側面においてもコンタクトが形成される。以下、このようなコンタクトをトップサイドコンタクトと称する。従来の構造において、トップサイドコンタクトを形成しようとすれば、層間絶縁物のエッチング工程によって、アイランド状珪素以外の部分の下地の酸化珪素膜、さらには、基板までエッチングされたが、本実施例では、窒化アルミニウム膜または窒化珪素膜２０２がエッチングストッパーとなって、ここでエッチングが止まる。

【００３６】通常の場合には、コンタクトホールの大きさは、ソース／ドレインよりも小さくする必要があったが、トップサイドコンタクトにおいては、逆にアイランドの大きさをコンタクトホールのよりも小さくでき、結果として、アイランドの微細化できる。また、逆にコンタクホールを大きくすることができるので、量産性、信頼性を高めることができた。

【００３７】最後に、水素中で３００～４００℃で０．１～２時間アニールして、珪素の水素化を完了した。このようにして、ＴＦＴを有する薄膜集積回路が完成した。そして同時に作製した多数のＴＦＴをマトリクス状に配列せしめ、かつ周辺回路をも同一基板上に形成した

モノシリック型のアクティブマトリクス型液晶表示装置とした。

【００３８】〔実施例３〕図１に示す多目的成膜装置を用いてＴＦＴを少なくとも一つ有する薄膜集積回路を作製する例を図３に示す。まず、本実施例において用いる多目的成膜装置について説明する。本実施例においては、１０１を基板の搬入搬出を行なうために予備室とした。また１０６を加熱を行なう処理室とし、１０３をプラズマＣＶＤ法によって窒化珪素膜を成膜する処理室とし、１０４をＴＥＯＳを原料としてプラズマＣＶＤ法により酸化珪素膜を成膜する処理室とし、１０５をＬＰＣＶＤ法により非晶質珪素膜を成膜する処理室とする。また、１０２をＰをドープした多結晶珪素膜を減圧熱ＣＶＤ法によって成膜する処理室とした。また各処理室には、各処理室を減圧状態にするための排気手段、さらには必要とされるガスを導入するためのガス導入手段が設けられている。

【００３９】以下に作製工程を示す。まず、基板としてＮＯガラスに代表される耐熱性の高い結晶化ガラス板（４インチ角、５インチ角または５×６インチ角）２０１を予備室１０１に搬入し、十分真空引きをする。この真空引きは、十分真空引きをされた搬送室１０７とほぼ同一の圧力になるまで行なうのが好ましい。そしてゲイトバルブ１１０を開け、ロボットアーム１０８によって、予備室１０１内の基板を搬送室１０７に移送する。図１においては、図３における基板２０１は１０９として示されている。なお、以下においてはその上に成膜されている膜も含めて基板という。そして、同じくほぼ同一圧力に真空引きがされた反応室１０３との間のゲイトバルブ１１２を開け、基板を搬入する。基板搬入後にゲイトバルブ１１２を閉め、この反応室１０３内において、窒化珪素膜２００をプラズマＣＶＤ法により、基板温度３５０℃、０．１Ｔｏｒｒ、SiH_4とNH_3との混合雰囲気で成膜する。この窒化珪素膜は基板からのアルカリの拡散を防ぐためである。

【００４０】そして、反応室１０３を真空引きし、ロボットアーム１０８によって、基板を再び真空引きがされた搬送室１０７に移送する。そして同じく真空引きがされた反応室１０６に基板を搬送する。この反応室１０６ではＴＥＯＳを原料としたプラズマＣＶＤ法で酸化珪素膜２０３が成膜される。成膜条件を以下に示す。

ＴＥＯＳ／O_2	＝１０／１００ｓｃｃｍ
ＲＦパワー	３５０Ｗ
基板温度	４００℃
成膜圧力	０．２５Ｔｏｒｒ

【００４１】また、上記反応において、C_2F_6を添加して、$SiOF_x$で示される膜を形成してもよい。

【００４２】この酸化珪素膜はＴＦＴを形成する面に下地酸化膜２０３として厚さ２０００～５０Åに成膜される。

【００４３】そして、再び基板を搬送室１０７に搬送し、次に反応室１０５に基板を搬入する。これら基板の移送の際において、搬送室とそれぞれの処理室とは同一真空度（同一減圧状態）に真空引きがされた上でゲイトバルブを開閉させることは全て共通である。

【００４４】反応室１０５では、ＬＰＣＶＤ法によって非晶質珪素膜２０４を２００～２０００Å、好ましくは３００～８００Å堆積する。ＬＰＣＶＤ法での成膜条件を以下に示す。

Si_2H_6	１００ｓｃｃｍ
Ｈｅ	２００ｓｃｃｍ
加熱温度	５００℃～５７０℃
成膜圧力	０．３Ｔｏｒｒ
グロースレート	５０Å～５００Å／分

【００４５】ここで、ジシランの如きポリシランを用いることは重要であって、これらを用い上記の条件で成膜することにより、その後の熱結晶化工程において２５０Å～８０００Åの平均粒径を有する特性の良い多結晶珪素膜を得ることができる。

【００４６】その後、処理の終了した基板は、搬出を行なうために予備室１０１に再び集められ装置の外部に取り出す。

【００４７】これは非晶質珪素膜２０４を島状にパターニングし、しかる後に結晶化させる為である。これは、これらのプロセスが減圧下におけるプロセスでないこと、およびこれらのプロセスに要する時間が他のプロセスに要する時間と比較して桁違いに長い為、装置の稼働率を高めるためには別の装置としたほうが効率的だからである。

【００４８】非晶質珪素膜２０４のパターニングは公知のフォトリソグラフィーを用いて所定のアイランド状にパターニングを行なう。

【００４９】熱結晶化は、窒素雰囲気中で５５０℃～６００℃で８時間から５６時間加熱することによって行う。この様に比較的低温で結晶化することにより、前述の様な大きな粒径の結晶を得ることができる。

【００５０】その後、ＮＯガラスの耐熱温度の範囲内で、出来るだけ高い温度、具体的には８００℃～８５０℃において熱アニールを行う。この工程によって、各結晶粒内の結晶性を向上させることが可能となる。また、この工程を酸化性雰囲気、例えばドライ酸素中で行い熱酸化膜を同時に形成しても良い。この熱酸化膜をゲート絶縁膜として用いる場合には、その膜厚は５００Å～２０００Åとすることが適当である。

【００５１】この様に結晶成長を終えた基板を、再び予備室１０１より装置内に投入する。

【００５２】予備室１０１より投入された基板は、必要に応じてさらに反応室１０４に基板を移送し、ＴＥＯＳを原料とするプラズマＣＶＤ法によって、図３（Ｂ）に示しように厚さ２００～１５００Å、好ましくは５００～１０００Åの酸化珪素膜２０５を形成する。ここでは、ＴＥＯＳを原料とし、酸素とともに基板温度３５０～６００℃、好ましくは３００～４５０℃で、ＲＦプラズマＣＶＤ法で分解・堆積した。ＴＥＯＳと酸素の圧力比は１：１～１：３、また、圧力は０．０５～０．５ｔｏｒｒ、ＲＦパワーは１００～２５０Ｗとした。

【００５３】この工程は、ＴＥＯＳを原料としてオゾンガスとともに減圧ＣＶＤ法もしくは常圧ＣＶＤ法によって、基板温度を３５０～６００℃、好ましくは４００～５５０℃として形成してもよい。

【００５４】また成膜後、酸素もしくはオゾンの雰囲気で４００～６００℃で３０～６０分アニールした。

【００５５】上記酸化珪素膜２０５の成膜は、熱結晶化後の高温アニールを酸化性雰囲気中で行い、熱酸化膜をゲート絶縁膜として使用する場合にはこの工程が不要になることは言うまでもない。

【００５６】かくして、図３（Ｂ）に示す如くガラス基板２０１上に窒化珪素のブロッキング層２０２、酸化珪素膜２０３、島状にパターニングされた結晶性珪素半導体膜２０４、酸化珪素膜２０５を多層に形成することができる。この図１に示す装置は、各チャンバーとロボットアームのある搬送室とはそれぞれゲイトバルブで仕切られているので、個々のチャンバー間において不純物が相互に混入することがなく、特に珪素膜中におけるＣ、Ｎ、Ｏの値を少なくなくと$5\times10^{19}cm^{-3}$以下とすることができる。

【００５７】上記ゲイト絶縁膜となる酸化珪素膜２０５を反応室１０４で成膜する場合は、その工程終了後、基板をアニール室１０６に搬入し、赤外線の照射によるラピットサーマルアニールをN_2、Ｏ雰囲気で行なうことは有効である。これは、酸化珪素膜２０５と珪素領域２０４との界面準位を減少させることに極めて効果がある。

【００５８】次に、上記ゲート絶縁膜の上にゲート電極となるＰをドープした多結晶珪素膜を減圧熱ＣＶＤによって１０００Å～４０００Åの厚さに形成する。

【００５９】上記の工程まで、即ち下地から珪素半導体層、ゲート絶縁膜、ゲート電極までの各界面が特に界面準位等に敏感でデバイスの特性を決定する主な部分であり、それ故に大気に暴露することなく連続的に成膜することが望ましく、本発明の構成によりそれが可能となる。

【００６０】以下の工程は本発明の装置から外部に搬出して行なう。

【００６１】まず、ゲート電極２１７を形成すべく、Ｐをドープした多結晶珪素膜をドライエッチングによりパターニングを行なう。（図３（Ｃ））

【００６２】その後、イオンドーピング法（プラズマドーピング法ともいう）によって、各ＴＦＴのアイランド状珪素膜中に、ゲイト電極２１７をマスクとして自己整合的に不純物（燐）を注入する。ドーピングガスとして

はフォスフィン（PH_3）を用いた。ドーズ量は、１～$4\times10^{15}cm^{-2}$とした。

【００６３】次に、基板を窒素雰囲気中で６００℃、１２時間加熱し、ドーパントの活性化を行なった後、さらに水素雰囲気中で４００℃、１時間熱処理し、水素化処理を行なって半導体層の欠陥準位密度を減少させる。

【００６４】その後、他の装置あるいは再び図１の装置を用い、全面に層間絶縁膜２１０を形成する。図１の装置を用いた場合には、図１の反応装置の反応室１０４を再び用い、ＴＥＯＳを原料として、これと酸素とのプラズマＣＶＤ法、もしくはオゾンとの減圧ＣＶＤ法あるいは常圧ＣＶＤ法によって酸化珪素膜を厚さ０．３μｍ～１μｍここでは３０００Å（０．３μｍ）形成した。基板温度は２５０～４５０℃、例えば、３５０℃とした。成膜後、表面の平坦性を得るため、この酸化珪素膜を機械的に研磨した。この工程は、図１の装置内に設けられた反応室を用いて等方性ドライエッチングを行なってもよい。さらに、スパッタ法によってＩＴＯ被膜を堆積し、これをパターニングして画素電極２１１とした。（図３（Ｅ））

【００６５】かくすると、電気光学装置の一方の基板側に薄膜集積回路を作ることができる。勿論、この図面に示す回路と同時に周辺回路を同一基板上に形成してもよい。そして、層間絶縁物２１０をエッチングして、図Ｆ（Ｅ）に示すようにＴＦＴのソース／ドレインにコンタクトホールを形成し、クロムもしくは窒化チタンの配線２１２、２１３を形成し、配線２１３は画素電極２１１に接続させた。なお、この際には、ソース／ドレイン領域（アイランド状珪素）をはみだしてコンタクトホールを形成してもよい。この場合にはコンタクトホールのうち、アイランド状珪素をはみだした面積は３０～７０％であった。この場合には、ソース／ドレインの上面のみならず、側面においてもコンタクトが形成される。以下、このようなコンタクトをトップサイドコンタクトと称する。従来の構造において、トップサイドコンタクトを形成しようとすれば、層間絶縁物のエッチング工程によって、アイランド状珪素以外の部分の下地の酸化珪素膜、さらには、基板までエッチングされたが、本実施例では、窒化珪素膜２００がエッチングストッパーとなって、ここでエッチングが止まる。

【００６６】通常の場合には、コンタクトホールの大きさは、ソース／ドレインよりも小さくする必要があったが、トップサイドコンタクトにおいては、逆にアイランドの大きさをコンタクトホールよりも小さくでき、結果として、アイランドの微細化ができる。また、逆にコンタクホールを大きくすることができるので、量産性、信頼性を高めることができた。

【００６７】このようにして、ＴＦＴを有する薄膜集積回路が完成した。そして同時に作製した多数のＴＦＴをマトリクス状に配列せしめ、かつ周辺回路をも同一基板上に形成したモノシリック型のアクティブマトリクス型液晶表示装置とした。

【００６８】尚、上記実施例において基板を石英基板とした場合には、下地の酸化珪素膜は省略可能であり、下地の酸化珪素膜も場合によっては省略してもよい。また、基板の耐熱性が高いために熱結晶化後の熱アニールあるいは熱酸化の工程の温度を１０００℃程度まで上昇させることが可能であり、その場合には更に結晶性の良い珪素膜を得ることが可能である。

【００６９】

【効果】本発明の構成を採用することで、基板上に多結晶珪素からなる半導体装置を作製する際に連続してプロセスをこなすことができ、生産性の向上、信頼性の向上を同時に果たすことができる。

【００７０】以上に説明した如く、図１のマルチチャンバー方式の多目的ＣＶＤ装置を用いることにより、図２（Ａ）の工程、ゲイト絶縁膜の形成、ＲＴＰ処理工程、層間絶縁膜の作製工程、とほとんど全ての工程を１台の装置で行なうことができる。そして、これらの工程は、マイクロコンピュータによって制御することができ、生産効率、コストパフォーマンスを向上させることができる。特に本発明装置を図２に示した如く結晶性ＴＦＴまたはこれを応用するモノシリック型薄膜集積回路へ応用することは著しい効果を得ることができる。

【図面の簡単な説明】

【図１】　実施例の多目的基板処理装置を示す。

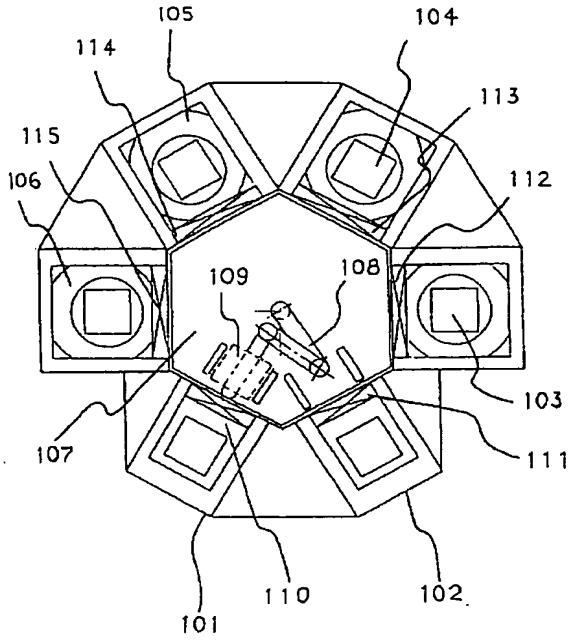
【図２】　実施例におけるＴＦＴの作製工程を示す。

【図３】　実施例におけるＴＦＴの作製工程を示す。

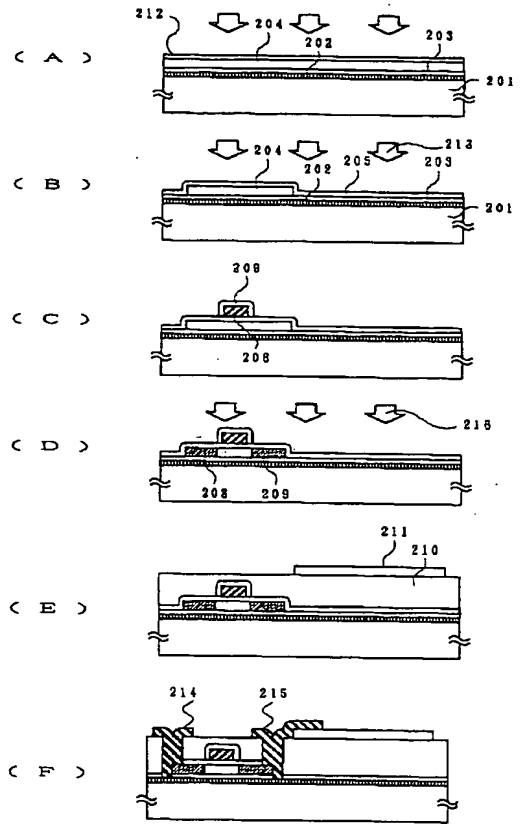
【符号の説明】

１０１～１０６・・・・処理室
１０８・・・・・・・・ロボットアーム
１０９・・・・・・・・基板
１１０～１１５・・・・ゲイトバルブ
２０１・・・・・・・・ガラス基板
２０２・・・・・・・・窒化アルミ膜
２００・・・・・・・・窒化珪素膜
２０３・・・・・・・・酸化珪素膜
２０４・・・・・・・・珪素膜
２０５・・・・・・・・酸化珪素膜（ゲイト絶縁膜）
２０６・・・・・・・・ゲイト電極
２０９・・・・・・・・陽極酸化物層
２１７・・・・・・・・ゲイト電極
２１０・・・・・・・・層間絶縁物
２１１・・・・・・・・ＩＴＯ電極（画素電極）
２１４／２１５・・・・ソース／ドレイン電極

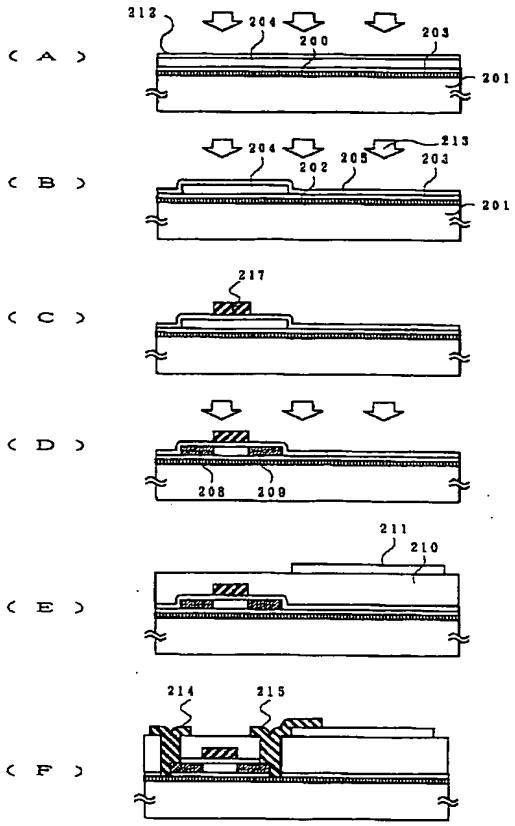
【図1】


105
104
114
113
115
106
112
109
108
103
107
111
110
102
101

【図2】


(A)
212
204
202
203
201
(B)
204
213
202
205
203
201
(C)
206
208
(D)
216
208
209
(E)
211
210
(F)
214
215

【図３】



フロントページの続き

(51)Int.Cl.[6]	識別記号	庁内整理番号	Ｆ Ｉ	技術表示箇所
Ｈ０１Ｌ　21/316		Ｘ　7352－4M		
21/318		Ｂ　7352－4M		

(72)発明者　阿部　寿
神奈川県厚木市長谷398番地　株式会社半導体エネルギー研究所内

【公報種別】特許法第１７条の２の規定による補正の掲載
【部門区分】第７部門第２区分
【発行日】平成１３年１０月１２日（２００１．１０．１２）

【公開番号】特開平７－１８３２３５
【公開日】平成７年７月２１日（１９９５．７．２１）
【年通号数】公開特許公報７－１８３３
【出願番号】特願平５－３４７６４６
【国際特許分類第７版】
H01L 21/205
C23C 16/24
16/40
16/44
16/50
H01L 21/316
21/318
【ＦＩ】
H01L 21/205
C23C 16/24
16/40
16/44 E
16/50
H01L 21/316 X
21/318 B

【手続補正書】
【提出日】平成１２年１２月２５日（２０００．１２．２５）
【手続補正１】
【補正対象書類名】明細書
【補正対象項目名】特許請求の範囲
【補正方法】変更
【補正内容】
【特許請求の範囲】
【請求項１】真空ポンプを備えた複数の処理室を有し、前記複数の処理室の一つは減圧熱ＣＶＤによる珪素膜の成膜室であり、前記複数の処理室の一つはプラズマＣＶＤによる酸化珪素膜または窒化珪素膜の成膜室であり、前記複数の処理室は真空ポンプを備えた共通室を介して連結されており、前記共通室は基板の搬送ロボットを有していることを特徴とするマルチチャンバ装置。
【請求項２】請求項１に記載されたマルチチャンバ装置は、光照射室、加熱室、スパッタリング室またはプラズマエッチング室を有していることを特徴とするマルチチャンバ装置。
【請求項３】請求項２において前記光照射は、赤外光照射またはエキシマレーザー光照射であることを特徴とするマルチチャンバ装置。
【請求項４】請求項１乃至請求項３のいずれか一項に記載されたマルチチャンバ装置の動作方法であって、前記複数の処理室の一つにて、成膜、加熱、光照射、またはエッチングしている時に、前記成膜、加熱、光照射、またはエッチングしている処理室とは異なる処理室にてプラズマクリーニングをすることを特徴とするマルチチャンバ装置の動作方法。
【請求項５】請求項４において前記プラズマクリーニングは、三フッ化窒素（ＮＦ，）ガスを用いていることを特徴とするマルチチャンバ装置の動作方法。
【請求項６】請求項１乃至請求項３のいずれか一項に記載されたマルチチャンバ装置の動作方法であって、前記複数の処理室の一つにおける室内の圧力と前記共通室における室内の圧力とが同一の時に、前記複数の処理室の一つに保持された基板を前記共通室に搬送することを特徴とするマルチチャンバ装置の動作方法。
【請求項７】請求項１乃至請求項３のいずれか一項に記載されたマルチチャンバ装置の動作方法であって、前記複数の処理室の一つにおける室内の圧力と前記共通室における室内の圧力とが同一の時に、前記共通室に保持された基板を前記複数の処理室の一つに搬送することを特徴とするマルチチャンバ装置の動作方法。
【請求項８】減圧熱ＣＶＤにより非晶質珪素膜を成膜する工程と、プラズマＣＶＤによりゲート絶縁膜を成膜する工程と、層間絶縁膜を成膜する工程と、前記非晶質珪素膜を結晶化する工程と、前記ゲート絶縁膜に光照射す

る工程とを複数の処理室を有するマルチチャンバ装置にて行うことを特徴とする薄膜集積回路の作製方法。
【請求項９】真空ポンプを備えた複数の処理室を有し、前記複数の処理室は真空ポンプを備えた共通室を介して連結されており、前記共通室は基板の搬送ロボットを有しているマルチチャンバ装置を用いた薄膜集積回路の作製方法であって、前記マルチチャンバ装置にて減圧熱ＣＶＤにより非晶質珪素膜を成膜し、前記非晶質珪素膜上にプラズマＣＶＤによりゲート絶縁膜を成膜し、前記ゲート絶縁膜に光照射した後に、前記非晶質珪素膜を結晶化することを特徴とする薄膜集積回路の作製方法。
【請求項１０】請求項８または請求項９において前記ゲート絶縁膜形成後の光照射は、赤外光照射であることを特徴とする薄膜集積回路の作製方法。
【請求項１１】請求項１０において前記赤外光照射を酸化二窒素（N_2O）ガス雰囲気中にて行うことを特徴とする薄膜集積回路の作製方法。
【請求項１２】請求項８または請求項９において前記非晶質珪素膜をエキシマレーザー光照射によって結晶化することを特徴とする薄膜集積回路の作製方法。
【手続補正２】
【補正対象書類名】明細書
【補正対象項目名】０００５
【補正方法】変更
【補正内容】
【０００５】
【課題を解決するための手段】多結晶珪素からなる活性層を有する半導体装置を特性良く作製するために、本発明の多目的基板処理装置は、複数の減圧可能な処理室を有し、前記複数の処理室は減圧可能な共通室を介して連結されており、前記共通室には各処理室間において基板を搬送するための手段を有し、前記複数の処理室の内の少なくとも一つは減圧熱ＣＶＤによる珪素膜の成膜が可能であり前記複数の処理室の内の少なくとも一つはプラズマＣＶＤによる酸化珪素膜あるいは窒化珪素膜の成膜が可能であること、あるいは、複数の減圧可能な処理室を有し、前記複数の処理室は減圧可能な共通室を介して連結されており、前記共通室には各処理室間において基板を搬送するための手段を有し、前記複数の処理室の内の少なくとも一つは減圧熱ＣＶＤによる珪素膜の成膜が可能であり前記複数の処理室の内の少なくとも一つはプラズマＣＶＤによる酸化珪素膜の成膜が可能であり、前記複数の処理室の内の少なくとも一つはプラズマＣＶＤによる窒化珪素膜の成膜が可能であることをその最も大きな特徴とする。
【手続補正３】
【補正対象書類名】明細書
【補正対象項目名】０００９
【補正方法】変更
【補正内容】
【０００９】本発明の具体的な例を図１に示す。図１に示す装置は多目的に利用できるものであって、必要とする成膜やアニール処理を施す処理室を必要とする数で組み合わせることができる。図１に示す装置で処理される基板としては、ガラス基板、シリコン基板、その他絶縁基板や半導体基板を用いることができる。即ち、絶縁表面を有する基板であれば用いることができる。例えば、アクティブマトリクス型の液晶表示装置やイメージセンサー等の電気光学装置であれば安価なガラス基板を用いるのが一般的である。
【手続補正４】
【補正対象書類名】明細書
【補正対象項目名】００５６
【補正方法】変更
【補正内容】
【００５６】かくして、図３（Ｂ）に示す如くガラス基板２０１上に窒化珪素のブロッキング層２０２、酸化珪素膜２０３、島状にパターニングされた結晶性珪素半導体膜２０４、酸化珪素膜２０５を多層に形成することができる。この図１に示す装置は、各チャンバーとロボットアームのある搬送室とはそれぞれゲイトバルブで仕切られているので、個々のチャンバー間において不純物が相互に混入することがなく、特に珪素膜中におけるＣ、Ｎ、Ｏの値を少なくとも５×１０^(18)ｃｍ^(-3)以下とすることができる。
【手続補正１】
【補正対象書類名】明細書
【補正対象項目名】００５６
【補正方法】変更
【補正内容】
【００５６】かくして、図３（Ｂ）に示す如くガラス基板２０１上に窒化珪素のブロッキング層２０２、酸化珪素膜２０３、島状にパターニングされた結晶性珪素半導体膜２０４、酸化珪素膜２０５を多層に形成することができる。この図１に示す装置は、各チャンバーとロボットアームのある搬送室とはそれぞれゲイトバルブで仕切られているので、個々のチャンバー間において不純物が相互に混入することがなく、特に珪素膜中におけるＣ、Ｎ、Ｏの値を少なくとも$5\times10^{18}cm^{-3}$以下とすることができる。